Ultra-Low-Power Biomedical Circuit Design and Optimization: Catching The Don't Cares

Xin Li, Ronald D. (Shawn) Blanton, Pulkit Grover and Donald E. Thomas
Electrical and Computer Engineering Department
Carnegie Mellon University
Pittsburgh, PA 15213, USA
{xinli, blanton, pgrover, thomas}@ece.cmu.edu

***Abstract*—To reduce healthcare cost while simultaneously delivering high-quality health services, developing new portable and/or implantable biomedical devices is of great importance for both health monitoring and clinical treatment. In this paper, we describe a radically new design framework for ultra-low-power biomedical circuit design and optimization. The proposed framework seamlessly integrates data processing algorithms and their customized ASIC implementations for co-optimization. The efficacy of the proposed framework is demonstrated by a case study of brain computer interfaces (BCIs).**

***Keywords*—Low power, biomedical circuit, optimization**

I. INTRODUCTION

As reported by United Nations [1] and US Census Bureau [2], the US population has enormously grown during the past several decades, climbing from 209 million in 1970 to 310 million in 2010. Most importantly, the percentage of senior citizens (more than 65-year old) is expected to reach 21.28% in 2050. With the rapid booming of senior citizen population, the expenditure of healthcare continuously increases at a rate of 5~10% per year in US [2]. Such a trend is also observed worldwide over a large number of other countries.

To reduce healthcare cost while simultaneously delivering high-quality health services, developing new portable and/or implantable biomedical devices is of great importance. Billions of US dollars could be saved by reforming today's healthcare infrastructure with these biomedical devices for various medical applications [3]-[5]:

- **Health monitoring**: Health condition should be reliably monitored for each person to predict and diagnose chronical diseases at the very early stage. For instance, ECG signals can be continuously measured and automatically classified by a portable biomedical device to diagnose arrhythmia [6]-[8].
- **Clinical treatment**: Clinical therapy should be reliably delivered for each patient for both preventative care and disease treatment. Taking neuroprosthesis as an example, brain signals can be sensed and decoded by an implantable device to control the prosthesis of a patient with neurological disorder [9]-[14].

Towards these goals, miniaturized portable and/or implantable biomedical circuits must be designed and deployed to reliably sense, process and transmit a large amount of physiological data with extremely low power consumption. These circuits must carry several important "features":

- **High accuracy**: A biomedical device must accurately generate the desired output (e.g., diagnosis result for arrhythmia [6]-[8], movement direction and velocity for neuroprosthesis [9]-[14], etc.) that is not contaminated by artifacts, errors and noises originated from human body and/or external environment [15]-[17].
- **Small latency**: The response of a biomedical device must be sufficiently fast for a number of real-time applications such as vital sign monitoring [18]-[19] and deep brain stimulation [20]-[21]. In these cases, physiological data must be locally processed within the biomedical device to ensure fast response time, especially when a reliable wired or wireless communication channel is not available to transmit the data to an external device (e.g., smart phone, cloud server, etc.) for remote processing. Even in the cases where data transmission is possible (e.g., neuroprosthesis control [9]-[14]), the raw data must be locally processed and compressed before transmission in order to minimize the communication energy.
- **Low power**: To facilitate a portable and/or implantable device to continuously operate over a long time without recharging the battery, its power consumption must be minimized. Especially for the implantable applications where power consumption is highly constrained (e.g., less than 100 μW), it is necessary to design an ASIC circuit, instead of relying on general-purpose microprocessors and/or programmable devices such as FPGAs, to meet the tight power budget [22]-[28].
- **Flexible reconfigurability**: Reconfigurability is needed to customize a biomedical device for different patients and/or different usage scenarios. For instance, the movement decoder of neuroprosthesis should be retrained every day to accommodate the time-varying characteristics of neural sources, recording electrodes and environmental conditions [14]. It, in turn, requires a reconfigurable circuit implementation that can be customized every day.

The aforementioned features, however, are considered to be mutually exclusive today. Taking neuroprosthesis as an example, executing a sophisticated movement decoding algorithm is overly power hungry for portable and/or implantable applications. For this reason, renovating the healthcare infrastructure with portable and/or implantable biomedical devices requires an even higher standard of performance than what can be offered by today's circuit technology.

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In this paper, we discuss a radically new design framework to seamlessly integrate data processing algorithms and their customized ASIC implementations for co-optimization. The proposed framework could bring about numerous opportunities to substantially improve the performance of biomedical circuits. From this point of view, it offers a fundamental infrastructure that enables next-generation biomedical circuit design and optimization for many emerging applications.

The remainder of the paper is organized as the follows. In Section II, we describe the proposed design framework, and then show a case study of brain computer interfaces (BCIs) in Section III. Finally, we conclude in Section IV.

II. How Can We Beat The State-Of-The-Art

In this paper, we attempt to address the following fundamental question: How can we further push the limit of accuracy, latency, power and reconfigurability to meet the challenging performance required for portable and/or implantable biomedical applications? Historically, algorithm and circuit designs have been considered as two separate steps. Namely, a biomedical data processing algorithm is first developed and validated by its software implementation (e.g., MATLAB, C++, etc.). Next, a circuit is designed to implement the given algorithm. Such a two-step strategy suffers from several major limitations that motivate us to fundamentally rethink the conventional wisdom in this area.

First, since the biomedical data processing algorithms are particularly developed and tuned for their software implementations, they are *not* fully optimized for circuit implementations. Ideally, data processing algorithms should be customized to mitigate the non-idealities induced by circuit implementations (e.g., nonlinear distortion of analog front-end, quantization error of digital computing, etc.). Second, while a circuit implementation inevitably introduces various non-idealities, these non-idealities can be classified into two broad categories: (i) *critical non-idealities* that may significantly distort the output of a biomedical circuit, and (ii) *non-critical non-idealities* that can be effectively mitigated or even completely eliminated by the data processing algorithm. A good circuit implementation should optimally budget the available resources (e.g., power) to maximally reduce the critical non-idealities rather than the non-critical ones.

Motivated by these observations, we propose to develop a radically new design framework to seamlessly *integrate* data processing algorithms and their customized ASIC implementations for co-optimization, as shown in Fig. 1. In this paper, we particularly focus on ASIC implementations (including analog, digital and mixed-signal circuits) in order to meet the tight power budget required by portable and/or implantable biomedical applications; however, it should be noted that the proposed design framework can be generally extended to other hardware platforms such as FPGAs.

Our core idea is to view a biomedical circuit, along with the data processing algorithm implemented by the circuit, as an information processing system. We develop an information theoretic metric, referred to as *information processing capacity* (IPC) that extends the conventional communication notion of channel capacity to our application of biomedical data sensing, processing and transmission. IPC quantitatively measures the amount of information that can be *processed* by the circuit. Intuitively, IPC is directly correlated to the accuracy of the circuit implementation. If a circuit can accurately process the input data and generate the desired output, its IPC is high. Otherwise, its IPC is low. In the extreme case, if a circuit cannot generate any meaningful output due to large errors, its IPC reaches the lowest value zero.

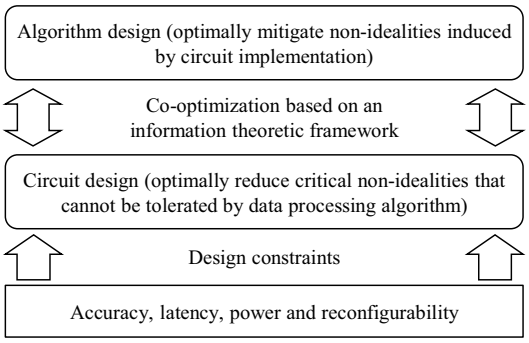

Fig. 1. An information theoretic framework is proposed to co-optimize data processing algorithms and their customized ASIC implementations for higher accuracy, smaller latency, lower power and better reconfigurability of biomedical devices.

IPC can efficiently distinguish critical vs. non-critical non-idealities. It is strongly dependent on the critical non-idealities that distort the output, and is independent of the non-critical non-idealities that can be eliminated by the data processing algorithm. Hence, it serves as an excellent "quality" metric that we should maximize in order to determine the optimal data processing algorithm and the corresponding circuit implementation subject to a set of design constraints (e.g., latency, power, reconfigurability, etc.).

It is important to note that our proposed design framework is *not* simply to combine algorithm and circuit designs. Instead, we aim to develop new methodologies that would profoundly revise today's data processing algorithms and integrated circuit designs for biomedical applications. In particular, our proposed information theoretic framework can optimally explore the tradeoffs between accuracy, latency, power and reconfigurability over all hierarchical levels from algorithm design to circuit implementation. From this point of view, the proposed framework based on IPC offers a fundamental infrastructure that enables next-generation biomedical circuit design and optimization for numerous emerging applications.

Due to the page limit, more details about IPC are not included in the paper. Instead, we will show a case study of BCIs to demonstrate the efficacy of the proposed design framework.

III. Case Study: Brain Computer Interface

Brain computer interface (BCI) has been considered as a promising communication technique for patients with neuromuscular impairments. For instance, neural prosthesis

provides a direct control pathway from brain to external prosthesis for paralyzed patients. It can offer substantially improved quality of life to these patients. To create a neural prosthesis, we must appropriately measure the brain signals and then accurately decode the movement information from the measured signals [9]-[14].

A variety of signal processing algorithms have been proposed for movement decoding in the literature. Most of these algorithms first extract the important features to compactly represent the information carried by the brain signals. Next, the extracted features are provided to a classification and/or regression engine to decode the movement information of interest. While most movement decoding algorithms in the literature are implemented with software on microprocessors, there is a strong need to migrate these algorithms to hardware in order to reduce the power consumption for practical BCI applications.

A. System Design

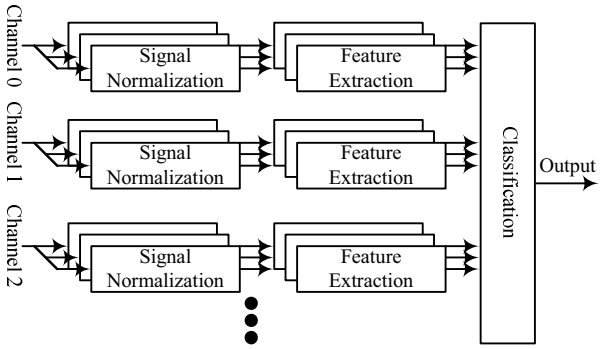

Fig. 2. A simplified block diagram is shown for the proposed hardware implementation of BCI.

Fig. 2 shows a simplified block diagram for the proposed hardware implementation of BCI. It consists of three major components:

- **Signal normalization**: The magnitude of brain signals varies from subject to subject and from channel to channel. Hence, representing brain signals by fixed-point arithmetic requires a large wordlength (i.e., a large number of bits). In order to minimize the wordlength and, consequently, the power consumption for fixed-point computation, we must appropriately normalize the brain signal from each channel.
- **Feature extraction**: There are many different feature extraction approaches for movement decoding of BCI. For instance, given the brain signal recorded from a particular channel, we can apply discrete cosine transform (DCT) and consider the DCT coefficients as the features for decoding [28].
- **Classification**: Once all features are extracted for multiple channels, they are further combined to decode the movement information. For instance, all features can be linearly combined by a linear classifier to determine the movement direction of interest. Here, a variety of linear classification algorithms (e.g., linear discriminant analysis, support vector machine, etc.) can be used, where the classifier training is performed offline. The on-chip classification engine performs the multiply-and-accumulate operations to determine the final output (i.e., the movement direction) from the features.

B. Experimental Results

We consider the ECoG data set collected from a human subject with tetraplegia due to spinal cord injury [14]. The ECoG signals are recorded with a high-density 32-electrode grid over the hand and arm area of the left sensorimotor cortex. The sampling frequency is 1.2 kHz. The human subject is able to voluntarily activate his sensorimotor cortex using attempted movements.

Our objective is to decode the binary movement direction (i.e., left or right) from a single trial that is 300 ms in length. The ECoG data set contains 70 trials for each movement direction (i.e., 140 trials in total). For movement decoding, 7 important channels with 6 features per channel (i.e., 42 features in total) are selected based on the Fisher criterion. A linear classifier is trained and implemented with 8-bit fixed-point arithmetic to decode the movement direction.

The BCI system is implemented with a Xilinx FPGA Zynq-7000 board. For testing and comparison purposes, we further implement a reference design based on the conventional technique [27]. In this sub-section, we compare the performance between our proposed hardware implementation and the reference design.

TABLE I
POWER AND ENERGY CONSUMPTION PER DECODING OPERATION

	Proposed Design	Reference Design
Power (mW)	0.72	3.8
Runtime (ms)	1.094	11.71
Energy (μJ)	0.787	44.5

TABLE II
POWER CONSUMPTION OF DIFFERENT FUNCTIONAL BLOCKS FOR THE PROPOSED DESIGN

Signal Normalization (μW)	25.2
Feature Extraction (μW)	690.2
Classification (μW)	2.6

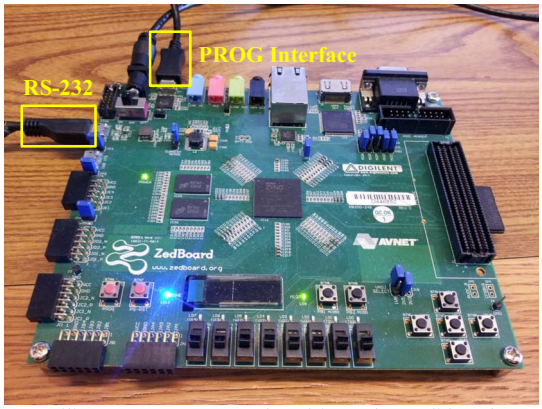

Fig. 3. A Xilinx FPGA Zynq-7000 board is used to validate the proposed hardware design for movement decoding of BCI.

We estimate the power and energy consumption for both the proposed and the reference designs by using Xilinx Power Analyzer, where the clock frequency is set to 0.5 MHz. Table I compares the power consumption for these two different

designs. Note that the proposed design achieves more than 56× energy reduction over the reference design. Table II further shows the power consumption for different functional blocks of the proposed design. Note that feature extraction dominates the overall power consumption for our proposed hardware implementation. Hence, additional efforts should be pursued to further reduce the power consumption of feature extraction in our future research.

To validate the proposed design on the Xilinx Zynq-7000 board, we first load our hardware design to the FPGA chip through the programming interface. Next, the ECoG data set is copied to an SD card that is connected to the Zynq-7000 board. When running the movement decoding flow, a single trial of the ECoG signals is first loaded to the SRAM block inside the FPGA chip. Next, these signals are passed to the functional blocks of signal normalization, feature extraction and classification for decoding. The decoding results are read back to an external computer through an RS-232 serial port on the Zynq-7000 board so that we can verify the decoding accuracy. Fig. 3 shows a photograph of the Xilinx FPGA Zynq-7000 board where the RS-232 port and the programming interface are both highlighted.

IV. CONCLUSIONS

In this paper, we describe a new design framework for ultra-low-power biomedical circuits. The key idea is to co-optimize data processing algorithms and their ASIC implementations based on an information theoretic metric: IPC. The proposed design framework has been demonstrated by a case study of BCIs. Our experimental results show that the proposed design achieves more than 56× energy reduction over a reference design. As an important aspect of our future research, we will further apply the proposed design framework to other emerging biomedical applications.

REFERENCES

[1] United Nations, *World Population Prospects: The 2006 Revision*, [Online] http://esa.un.org/wpp/.

[2] US Census Bureau, *Health & Nutrition: Health Expenditures*, [Online] http://www.census.gov/compendia/statab/cats/health_nutrition/health_expenditures.html.

[3] Gary and Mary West Wireless Health Institute, "Wireless Solutions for Health Care Reform," http://www.westhealth.org/sites/default/files/wwhi_white_paper.pdf.

[4] X. Teng, et. al., "Wearable medical systems for p-health," *IEEE Reviews in Biomedical Engineering*, vol. 1, pp. 62-74, Dec. 2008.

[5] J. Ko, et. al., "Wireless sensor networks for healthcare," *Proceedings of The IEEE*, vol. 98, no. 11, pp. 1947-1960, Nov. 2010.

[6] S. Osowski, et. al., "Support vector machine-based expert system for reliable heartbeat recognition," *IEEE Trans. on Biomedical Engineering*, vol. 51, no. 4, pp. 582-589, Apr. 2004.

[7] P. Chazal and R. Reilly, "A patient-adapting heartbeat classifier using ECG morphology and heartbeat interval features," *IEEE Trans. on Biomedical Engineering*, vol. 53, no. 12, pp. 2535-2543, Dec. 2006.

[8] C. Ye, et. al., "Heartbeat classification using morphological and dynamic features of ECG signals," *IEEE Trans. on Biomedical Engineering*, vol. 59, no. 10, pp. 2930-2941, Oct. 2012.

[9] G. Pfurtscheller and C. Neuper, "Motor imagery and direct brain-computer communication," *Proceedings of The IEEE*, vol. 89, no. 7, pp. 1123-1134, Jul. 2001.

[10] E. Leuthardt, et al., "A brain-computer interface using electrocorticographic signals in humans," *Journal of Neural Engineering*, vol. 1, no. 2, pp. 63-71, Jun. 2004.

[11] M. Lebedev and M. Nicolelis, "Brain-machine-interface: past, present and future," *Trends in Neurosciences*, vol. 29, no.9, pp.536-546, Sep. 2006.

[12] A. Schwartz, et al., "Brain-controlled interfaces: movement restoration with neural prosthetics," *Neuron*, vol. 52, no. 1, pp. 205-220, Oct. 2006.

[13] J. Donoghue, "Bridging the brain to the world: a perspective on neural interface systems," *Neuron*, vol. 60, no. 3, pp.511-521, Nov. 2008.

[14] W, Wang, et. al., "An electrocorticographic brain interface in an individual with tetraplegia," *Plos One*, vol. 8, no. 2, Feb. 2013.

[15] N. Thakor and Y. Zhu, "Applications of adaptive filtering to ECG analysis: noise cancellation and arrhythmia detection," *IEEE Trans. on Biomedical Engineering*, vol. 38, no. 8, pp. 785-794, Aug. 1991.

[16] K. Nazarpour, et. al., "Removal of the eye-blink artifacts from EEGs via STF-TS modeling and robust minimum variance beamforming," *IEEE Trans. on Biomedical Engineering*, vol. 55, no. 9, pp. 2221-2231, Sep. 2008.

[17] C. Guo, et. al., "Real-time robust signal space separation for magnetoencephalography," *IEEE Trans. on Biomedical Engineering*, vol. 57, no. 8, pp. 1856-1866, Aug. 2010.

[18] K. Yousef, et. al., "Characteristics of patients with cardiorespiratory instability in a step-down unit," *American Journal of Critical Care*, vol. 21, no. 5, pp. 344-350, Sep. 2012.

[19] S. Khalid, et. al., "A two-class approach to the detection of physiological deterioration in patient vital signs with clinical label refinement," *IEEE Trans. on Information Technology in Biomedicine*, vol. 16, no. 6, pp. 1231-1238, Nov. 2012.

[20] M. Kringelbach, et. al., "Translational principles of deep brain stimulation," *Nature*, vol. 8, pp. 523-635, Aug. 2007.

[21] C. Oluigbo, et. al., "Deep brain stimulation for neurological disorders," *IEEE Reviews in Biomedical Engineering*, vol. 5, pp. 88-99, 2012.

[22] X. Zou, et. al., "A 1-V 450-nW fully integrated programmable biomedical sensor interface chip," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1067-1077, Apr. 2009.

[23] R. Muller, et. al., "A 0.013 mm^2, 5 μW, DC-coupled neural signal acquisition IC with 0.5 V supply," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 1, pp. 232-243, Jan. 2012.

[24] C. Lopez, et. al., "A multichannel integrated circuit for electrical recording of neural activity, with independent channel programmability," *IEEE Trans. on Biomedical Circuits and Systems*, vol. 6, no. 2, pp. 101-110, Apr. 2012.

[25] K. Lee, et. al., "Low-energy formulations of support vector machine kernel functions for biomedical sensor applications," *Journal of Signal Processing Systems*, vol. 69, no. 3, pp. 339-349, Dec. 2012.

[26] E. Winokur, et. al., "A wearable cardiac monitor for long-term data acquisition and analysis," *IEEE Trans. on Biomedical Engineering*, vol. 60, no. 1, pp. 189-192, Jan. 2013.

[27] J. Yoo, et al., "An 8-channel scalable EEG acquisition SoC with patient-specific seizure classification and recording processor," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 1, pp. 214-228, Jan. 2013.

[28] M. Won, et. al., "Low-power hardware implementation of movement decoding for brain computer interface with reduced-resolution discrete cosine transform," *IEEE EMBC*, 2014.