Error Characterization, Mitigation, and Recovery in Flash Memory Based Solid-State Drives

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I. Introduction

In this work, we provide a comprehensive overview of the state of flash memory based SSD reliability, with a focus on (1) fundamental causes of flash memory errors, backed up by (2) quantitative error data collected from real state-of-the-art flash memory devices, and (3) sophisticated error mitigation and data recovery techniques developed to tolerate, correct, and recover from such errors.

II. State-of-the-Art SSD Architecture

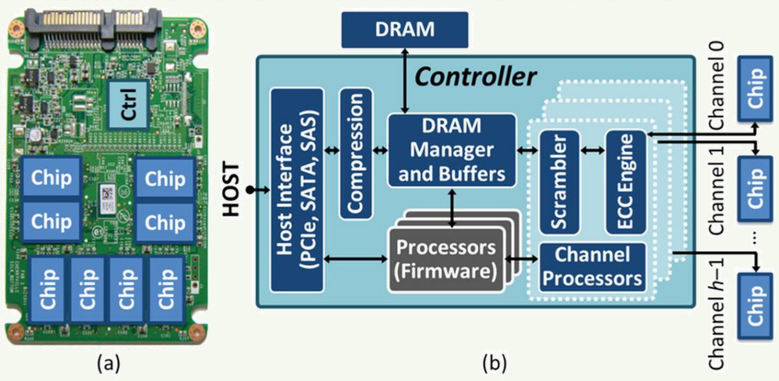


Figure 1. (a) SSD system architecture, showing controller (*Ctrl*) and chips; (b) detailed view of connections between controller components and chips.

II.C. SSD Controller

Flash Translation Layer, Flash Reliability Management, Compression, Data Scrambling and Encryption, Error-Correcting Codes, Data Path Protection, Bad Block Management, Superpage-Level Parity

II.D. Design Trade-offs for Reliability

Trade-off Between Write Amplification and Overprovisioning, Trade-off Between P/E Cycle Endurance and Overprovisioning

III. NAND Flash Memory Basics

Storing Data in a Flash Cell, Flash Block Design, Read Operation, Program and Erase Operations

IV. NAND Flash Error Characterization

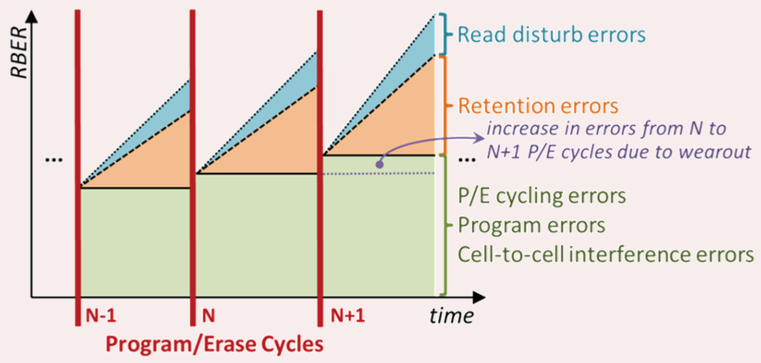


Figure 12. Pictorial depiction of errors accumulating within a NAND flash block as P/E cycle count increases.

Threshold Voltage Distribution for:
P/E Cycling Errors, Data Retention Errors, and Read Disturb Errors

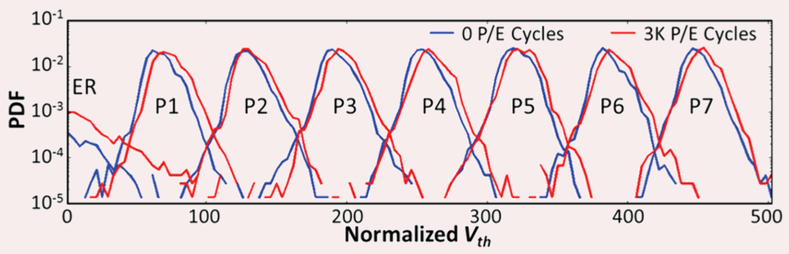
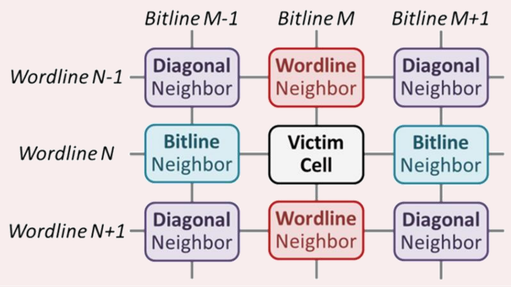


Figure 14. Threshold voltage distribution of TLC NAND flash memory after 0 P/E cycles and 3K P/E cycles.

Also Discussed: Program Errors,
Cell-to-Cell Program Interference Errors, and Large-Scale Studies on SSD Errors



Process Technology	Wordline Neighbor	Bitline Neighbor	Diagonal Neighbor
2y-nm	0.060	0.032	0.012
1x-nm	0.110	0.055	0.020

Table 2. Coupling coefficients for immediately-adjacent cells.

V. Error Mitigation

Mitigation Mechanism	*P/E Cycling* [32,33,42] (§IV.A)	*Program* [40,42,53] (§IV.B)	*Cell-to-Cell Interference* [35,36,55] (§IV.C)	*Data Retention* [20,32,34,37,39] (§IV.D)	*Read Disturb* [20,32,38,62] (§IV.E)
Shadow Program Sequencing [35,40] (Section V.A)			X		
Neighbor-Cell Assisted Error Correction [36] (Section V.B)			X		
Refresh [34,67,68] (Section V.C)				X	X
Read-Retry [33,72] (Section V.D)	X			X	X
Voltage Optimization [37,38,74] (Section V.E)	X			X	X
Hot Data Management [41,63,70] (Section V.F)	X	X	X	X	X
Adaptive Error Mitigation [43,65,77,78,82] (Section V.G)	X	X	X	X	X

Table 3. List of different types of errors mitigated by NAND flash error mitigation mechanisms.

Shadow Program Sequencing

Neighbor-Cell Assisted Error Correction

		BL0	BL1	BL2	BL3	BL4	BL5	BL6	BL7
Originally-programmed value		11	00	01	10	11	00	01	00
1. Read (using V_{opt}) with *errors*		01	00	00	00	11	10	00	01
NAC	2. Read **adjacent wordline**	P2	ER	P2	ER	P1	P3	P1	ER
NAC	3. *Correct cells* adjacent to ER	01	00	00	***10***	11	10	00	***00***
NAC	4. *Correct cells* adjacent to P1	01	00	00	10	11	10	***01***	00

Figure 21. Overview of neighbor-cell assisted error correction.

Refresh Mechanisms

- Remapping-Based Refresh, In-Place Refresh, Read Reclaim, Adaptive Refresh and Read Reclaim Mechanisms

Read-Retry

Voltage Optimization

- **Optimizing Read Reference Voltage**

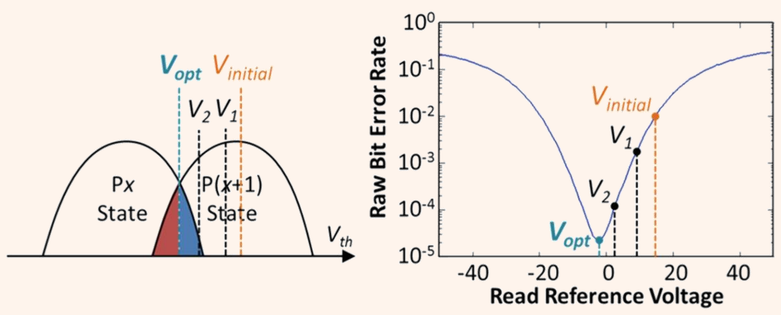


Figure 23. Finding the optimal read reference voltage after the threshold voltage distributions overlap (left), and raw bit error rate as a function of the selected read reference voltage (right).

- **Optimizing Pass-Through Voltage**

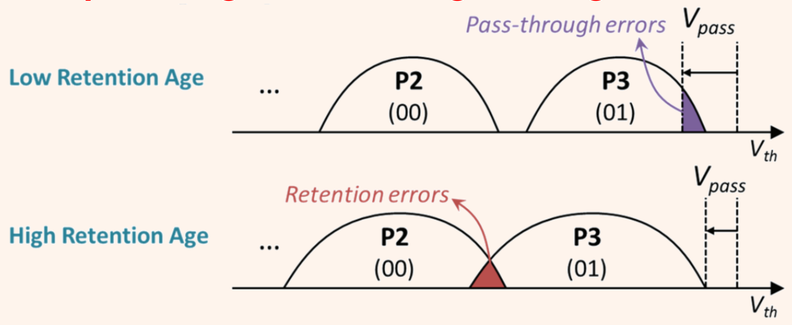


Figure 25. Dynamic pass-through voltage tuning at different retention ages.

Hot Data Management

Adaptive Error Mitigation Mechanisms

- **Multi-Rate ECC**, Dynamic Cell Levels

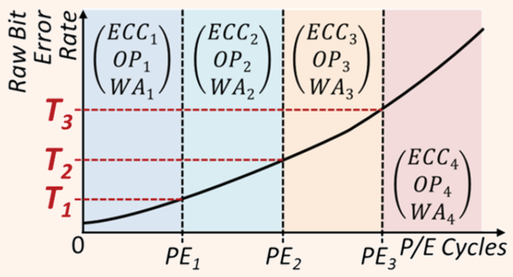


Figure 27. Illustration of how multi-rate ECC switches to different ECC codewords (i.e., ECC_i) as the RBER grows. OP_i is the overprovisioning factor used for engine ECC_i, and WA_i is the resulting write amplification value.

VI. Error Correction and Data Recovery

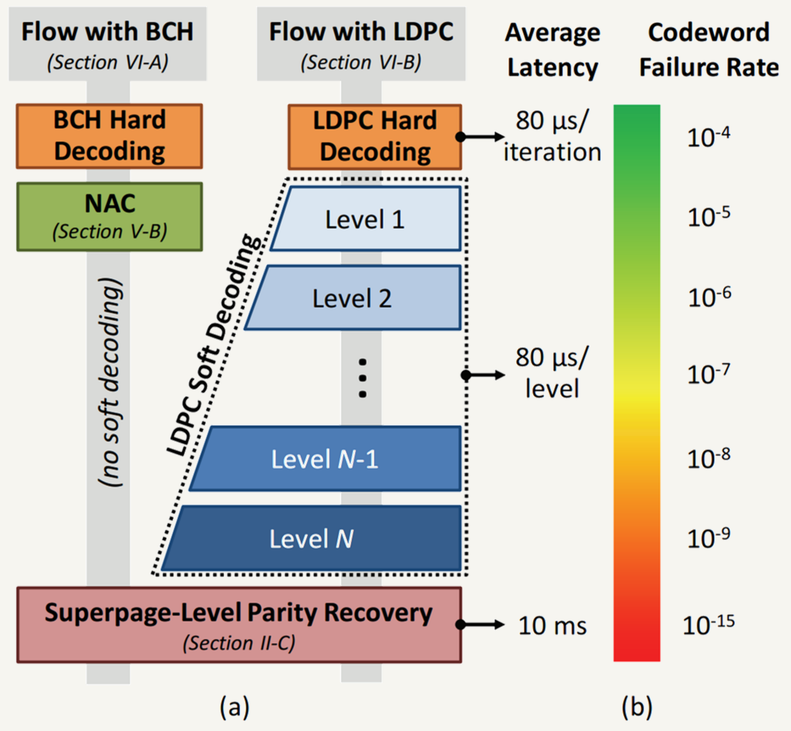


Figure 30. (a) Example error correction flow using *BCH codes* and *LDPC codes*; (b) the corresponding average latency and codeword failure rate for each LDPC stage.

Error Correction Flow with LDPC Codes

- Soft Decoding
- Computing LLR Values
- Determining the Number of Soft Decoding Levels

BCH and LDPC Error Correction Strength

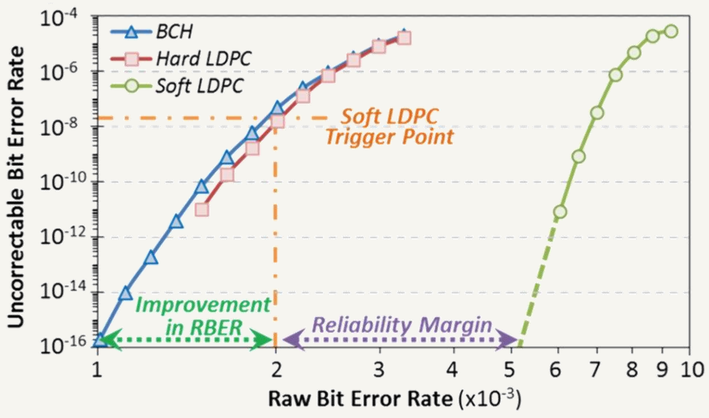


Figure 32. Raw bit error rate vs. uncorrectable bit error rate for BCH codes, hard LDPC codes, and soft LDPC codes.

SSD Data Recovery

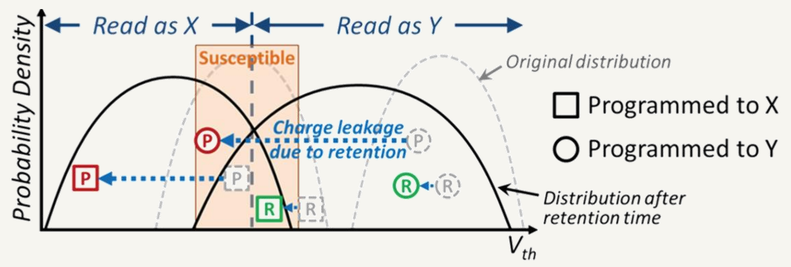


Figure 33. Some retention-prone (P) and retention-resistant (R) cells are incorrectly read after charge leakage due to retention time. Retention Failure Recovery (RFR) identifies and corrects the incorrectly-read cells based on their leakage behavior.

VII. Emerging Reliability Issues for 3D NAND Flash

VIII. Similar Errors in Other Memory Technologies

- Data Retention Errors in DRAM
- Cell-to-Cell Interference Errors in DRAM
- Read Disturb Errors in DRAM
- Large-Scale DRAM Error Studies
- Latency-Related Errors in DRAM
- Error Correction in DRAM
- Errors in Emerging Non-Volatile Memory Technologies

Appendix: TLC Threshold Voltage Distribution Data

Scan QR Code (top right corner) to download the full paper
(https://arxiv.org/pdf/1706.08642.pdf)

Y. Cai et al. *Error Characterization, Mitigation, and Recovery in Flash Memory Based Solid State Drives*. Proc. of the IEEE, Sept. 2017.

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