Design Automation for Analog: The Next Generation of Tool Challenges

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ABSTRACT

The decade of the 1990s saw the first wave of practical "post-SPICE" tools for analog designs. A range of synthesis, optimization, layout and modeling techniques made their way from academic prototypes to first-generation commercial offerings. We offer some pragmatic prognostications for what the next wave might (or, more bluntly, *should*) focus on next, as pressure to improve AMS design productivity grows.

Categories and Subject Descriptors

B.7.2 [**Integrated Circuits**]: Design Aids

General Terms

Analog, Algorithms, Design, Synthesis.

Keywords

Analog, mixed-signal, integrated circuits, computer-aided design

1. INTRODUCTION

Over the last roughly half dozen years, analog design automation tools "got real" in one important sense: a range of synthesis, optimization, modeling and layout tools moved from concept demonstrations (most commonly academic) to first-generation, supported commercial offerings. We refer to these as "post-SPICE" tools; this is convenient shorthand for one unifying characteristic of these tools – the characteristic of interest in this paper – the fact that they were *not* simulation tools. To be sure, simulators saw significant advances as well in this time frame. But for the first time, we also saw some tools specifically aimed at synthesis and optimization emerge, for sizing, for centering, for layout, and so forth.

Several recent publications survey this current terrain nicely [1-3]. Based on our own experiences, with the CMU analog toolset [4-6] and its industrial progeny [7-9] we offer the following as the essential components of the current state of the art:

- **Simulation-based sizing synthesis:** these tools support circuit-level sizing, biasing, and centering. They employ global numerical optimization techniques for robustness, and network-of-workstations parallelism for speed. The key idea is full SPICE-level simulation for each solution candidate proposed during optimization. The strategy has two key virtues: it can be used for any design (i.e., any fixed topology) that one can simulate; and it produces designs that pass designer-provided simulation scripts. These tools optimally reuse the verification infrastructure that all circuit designers already build for each circuit they create. And it produces "trustworthy" results, since one can immediately see that they simulate correctly, using the designer's own simulator.
- **Optimization-based layout:** these tools replicate at device level what ASIC-level floorplanning, placement, and routing tools do at chip level. The key components are a library of generators for common device-level analog structures (e.g., analog PCELLS), and device-level placement and shape-level routing tools sensitive to analog issues such as symmetries, crosstalk and parasitic balance.

There are several examples of successes at the analog cell level (comprising roughly 10-100 devices) using these sorts of tools; Figure 1 shows one synthesis experiment from [7].

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2. CHALLENGES: NEXT GENERATION

So, if we have first-generation of tools for cell-level analog designs, what's next? Herewith, a *short* list of *big* challenges.

2.1 Integration

Neither designers, nor tools, exist in a vacuum. By "integration" we mean the process by which tools, GUIs, database schemas, usage models, etc., *co-evolve* to become maximally useful to working designers. For simulation tools, we have seen huge improvements from this co-evolution process: point tools for schematic capture, netlisting, simulation, waveform viewing, shapes-level layout, cross-probing, etc., are highly integrated today. This was certainly *not* the case when these tools appeared in the late 1980s. Similarly, the introduction of logic synthesis tools ultimately caused significant changes in the surrounding

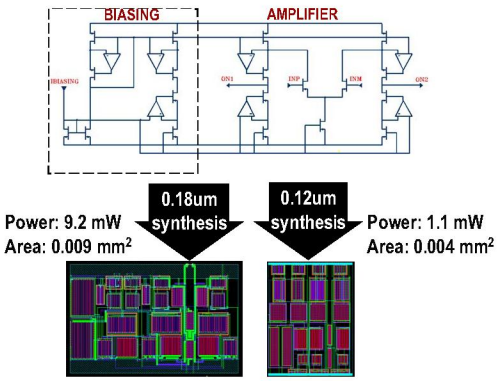

Figure 1. Example of industrial cell-level sizing/layout synthesis, from circuit experiments of [7].

RTL infrastructure; a good example is the emergence of synthesizable subsets of Verilog and VHDL.

We are still at the beginning of this co-evolution process for the post-SPICE analog tools. It is unfortunate that this process is underappreciated in academic circles, and regarded as uncreative spade-work down in the trenches of database fields and glue scripts. However, the integration process is often the make-or-break step in the path from concept to widespread adoption. A critical case in point here is the management of analog design constraints.

2.2 Constraint Extraction/Management/Reuse

Optimization-based tools have an uncanny knack for producing horrendous results when they are inappropriately set up. This is especially true for analog circuits and layouts, where even designs with a small number of elements may be subject to a large number of critical constraints. This complexity of constraints in the analog and mixed-signal world presents both challenges and opportunities.

Consider a typical analog design team, comprising a mix of circuit engineers and layout technicians. If the team has been working together for some time, and has a portfolio of successful prior designs, it has almost certainly evolved a detailed vocabulary for specifying critical topological, electrical, geometric, thermal, etc., constraints. The good news (for the team, anyway), is that such information exists. The bad news for those of us in the CAD business is that *this information is almost never written down*. Worse, when it is, its form differs from team to team, product to product, and company to company.

Extracting this information is essential for many reasons. We need it to drive our synthesis and optimization tools. (Indeed, we have lots of evidence [4-9] that when properly constrained, these tools can produce excellent, competitive designs.) We need it to parameterize error checking functions. We need it if we ever hope to make reusable IP for analog circuits. In short, we need this information to evolve a design environment with a seamless spectrum of design entry, design editing, design synthesis/optimization, design verification, and design reuse tools for the analog and mixed-signal universe.

This problem features many of the things that make CAD work really challenging: it's ill-defined, crosses abstraction boundaries (electrical, geometric, hierarchical), and needs to be parameterizable to adapt to different design styles, design groups, designed products. And, best of all, if we fail to do it right, our beautiful first-generation synthesis tools will all end up gathering dust in a corner somewhere, while our overworked analog design colleagues retreat back to manual editors and lots and lots of SPICE jobs.

Some of the work to be done is "integration" as discussed previously. We need to lower the barriers to entry of these constraints, making them a natural and expected part of the design process. This work will happen in the commercial sphere. OpenAccess [10], the open source industry-wide database initiative is a very important step in this direction.

However, there is also opportunity for longer range fundamental research. Take any complex circuit schematic/layout from a high-performing analog team, and ask "*what's critical about this design*?". One will be amazed at the density of information encoded in a few essential annotations, or a small set of critical simulation waveforms. The goal is to be able extract these kinds of implicit "meta-constraints" *without* having to bother the designer. It's a serious, exciting analog CAD challenge.

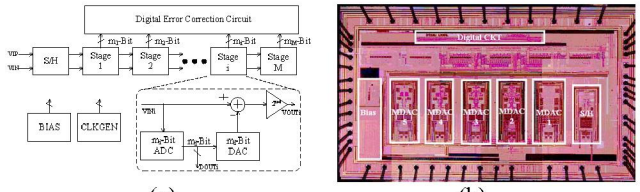

Figure 2. Hybrid AMS design using top-level analytical models with cell-level simulation-based synthesis, from [13]. (a) Overall pipelined ADC architecture. (b) Final 13b 40MS/s ADC layout, 364mW, 73.8dB SNR in 0.25um 3.3V TSMC CMOS.

2.3 System Design/Exploration/Optimization

The emerging first generation of analog synthesis/optimization tools targets cell-level designs in the range of 10-100 devices. One significant reason is the use of simulation-based optimization, which visits many design candidates and simulates each one at full SPICE-level.

At system level, we may have 10-100 fundamental circuit *blocks*, not transistors. We cannot simulate these designs flat at the device level very efficiently. So-called "fast SPICE" engines make flattened simulation times more bearable, but still don't support the thousands of candidate evaluations that simulation-based optimization loops rely upon. Attempts to bypass the simulation-based strategies, e.g., by using all-analytical equation-based descriptions based on convex (and thus easily optimized) descriptions (e.g., [11]), proved to be a dead end. The convex models are mathematically elegant, but too expensive to build for each new circuit, and too inaccurate versus detailed simulation.

So, what are the important tool challenges to be addressed here? Much of system level design is about trade-off analysis, understanding if a system architecture is correct, and how far it can be pushed – *before* one has fully designed it. Can we help designers make the best trade-off decisions, up at this much less concrete level of design detail? Can we help refine a design candidate to transistor level more quickly, to see if any of the components are too intractable (or too risky) to design? *These* are challenging and interesting analog optimization problems.

There are a variety of evolving approaches in this area. Hybrid schemes are one strategy worth mention. These use simulation-based synthesis engines but mix circuit level simulations for key cells with analytical formulations for top-level design tradeoffs. The work of Mukherjee et al. in [12-13] is one nice example, illustrated in Figure 2. They show how to use these ideas to explore architecture alternatives for a pipelined ADC under tight power goals, and how to synthesize components for an optimal circuit design once an a optimal architecture has been selected.

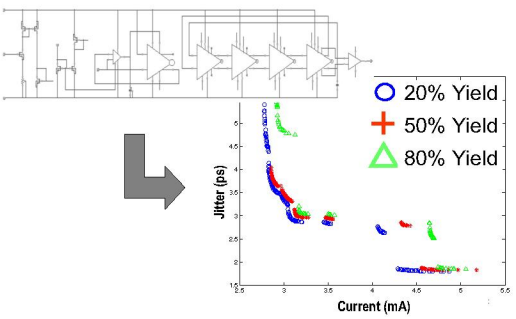

Figure 3. Statistical Pareto tradeoff curves from [16], show statistically achievable VCO current (i.e., power) vs. jitter .

Another strategy strives to extract explicit component level tradeoffs – *Pareto* surfaces – and use these tradeoff curves as the basis for efficient optimization at system level [14-16].

In general, this remains a rather open problem. We need flexible methods that are not only tractable, but also attractive to practicing system designers who rely almost exclusively on fast simulation. We need work not only on optimization and modeling, but also on the integration and constraint management consequnces of these algorithms.

2.4 Statistical AMS Design

It should come as no surprise that designing analog, RF and mixed-signal circuits in increasingly scaled digital technologies poses new CAD challenges. The devices we will be using are increasingly subject to a wide range of both systematic and random perturbations. Their resulting performance characteristics are not only poor for many analog purposes (e.g., gain is very low) but also distributed much more widely about the nominal mean parameter values.

Most of the first-generation tools evolved to attack nominal design problems. Most of the simulation-based sizing engines can be (or, have been) married with various Monte Carlo strategies to address, at least to first order, the statistical case. However, in our opinion, we are still just scratching the surface here. We mention two specific opportunities.

One area is *circuit/layout co-design*. It is already true that the most high-performance circuits are implicitly co-designed: layout decisions, for matching, for isolation, for cross-talk, etc., are being juggled from the moment the circuit topology is defined and sizing begins. Formulating this as an explicit co-design problem seems a very attractive – and computationally challenging – problem.

Another area is *statistical system-level design*. Most synthesis experiments at system-level have targeted the nominal case, since statistical variation is difficult to capture in large scale optimization. There are many interesting strategies emerging. Our recent work at CMU [16] uses cell-level synthesis to built *statistical tradeoff curves*: tradeoff surfaces that "guarantee" that, under statistical parameter variation, some prescribed fraction (a yield level) for a given performance level. Figure 3 shows one such statistical Pareto curve. Other approaches is deterministic optimization strategies to maximize *design margins* for approximate versions of the system level problem [17], or extend *response surface methods* to high dimensional, highly correlated statistical scenarios [18]. Much remains to be done, when dealing with system designs and at the same time, statistically varying components.

3. SUMMARY

A first generation of post-SPICE synthesis/optimization tools is currently making the transition to industrial use. We suggest four areas as priorities for next-generation work: careful integration, painless constraint extraction, practical system-level design assistance, and statistical design for circuits, layouts, and systems. These four areas comprise a *short* list of *big, open* problems in analog CAD.

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