Execute with picture + peak performance
- 1/4 to 3/4 microinstructions

Show: 1/4 to cases

Note: flowchart (hp) is given in a nonstandard way.
- Cache structure \( 2^{14} \times 8 \\
- 16k \times 4\) way set associative cache
- address (bytewise)
- cache line \( 2^6 = 64B \)

- 2\(^2 \) associativity

- CRU replacement

- Explain cache misses (compulsory, capacity, conflict)
- Accessing a vector in unit stride
- Accessing a vector in 2-power stride
- 1 data \( \rightarrow 8 \) stored in cache, \( \frac{8}{N} \) CRU's for vector length
- Accessing a 2D array