WSB: RF Reconfiguration Using Phase-Change Switches

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• Dedicated transceiver (or at least dedicated front-end) for each band/standard
Wideband Multiband XCVR (research)

- Lots of new interesting research in all-CMOS wideband, interference-tolerant RX front-ends
- Many new digital-friendly TX architectures
  - But these are all still narrowband
  - Many still require off-chip filtering to meet spectral mask
Reconfigurable Multiband XCVR

- Frequency reconfigurable blocks
- Need high quality switches with low $R_{ON}$ and $C_{OFF}$, and high $R_{OFF}$
  - Via switches using CMOS-compatible PC materials
FPRA: Towards an RF “FPGA”

• Similar concept to digital FPGA’s
• Need nearly ideal switches to realize this concept

Phase-Change Materials

- Proposed for non-volatile memories in early 1960’s by Ovshinsky
- Material: Chalcogenides $\text{Ge}_x\text{Sb}_y\text{Te}_z$, e.g., GST, GeSb
- Applications
  - CMOS-based non-volatile memories
  - NV-RAM
  - Re-writeable DVD’s and CD’s (contrast in reflectivity)

Phase Transformation

- \( R_{OFF}/R_{ON} \approx 10^3 \) to \( 10^7 \).
- To transform to crystalline (\( R_{ON} \))
  - Heat PC material above crystallization temperature
  - Allow PC material to cool gradually, allowing it to crystallize
- To transform to amorphous (\( R_{OFF} \))
  - Heat PC material above melting temperature
  - Quench (Cool) PC material rapidly, allowing no time for crystallization
- Transformation is reversible
Phase-Change Vias

- PC cells commonly used in non-volatile memories
- Typically implemented low in metal stack
e.g., between transistor contact and M1

Unsuitable for RF reconfiguration because of series heater


1st Generation CMU PC Via Structure

- State of phase-change via makes or breaks connection between nodes A & B
- Thick top metal for low trace resistance
- Structure necessary for transformation in RF

1st Generation CMU PC Via

<table>
<thead>
<tr>
<th>Material</th>
<th>$\rho_{OFF}/\rho_{ON}$</th>
<th>$\rho_{ON}$ (Ω-m)</th>
<th>$\varepsilon_r$</th>
</tr>
</thead>
<tbody>
<tr>
<td>GeTe</td>
<td>$2.5 \times 10^6$</td>
<td>$4 \times 10^{-6}$</td>
<td>$\approx 18$</td>
</tr>
</tbody>
</table>

Intrinsic via model

Via model with parasitics
### PC Vs CMOS

<table>
<thead>
<tr>
<th>NMOS Tech. node (nm)</th>
<th>Width (μm)</th>
<th>$R_{ON,\text{triode}}$ (Ω)</th>
<th>$R_{ON,\text{large}}$ (Ω)</th>
<th>$C_{OFF}$ (fF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>130</td>
<td>794</td>
<td>0.811</td>
<td>4.24</td>
<td>800</td>
</tr>
<tr>
<td>90</td>
<td>698</td>
<td>0.792</td>
<td>3.23</td>
<td>348</td>
</tr>
<tr>
<td>65</td>
<td>383</td>
<td>0.813</td>
<td>3.1</td>
<td>177</td>
</tr>
<tr>
<td>45</td>
<td>300</td>
<td>0.807</td>
<td>2.89</td>
<td>108.4</td>
</tr>
<tr>
<td>32</td>
<td>293</td>
<td>0.804</td>
<td>2.63</td>
<td>102.7</td>
</tr>
</tbody>
</table>

- **GeTe via**: 0.4, 1.6
- **GeTe-via switch**: 0.8, 6.5
PC Vs CMOS: Switch Bandwidth

\[ f_{SW} = \frac{1}{2\pi RC} \]

Switch Bandwidth (THz) vs Technology nodes (nm)

PC switch

\[ C = 30.6 \]

Technology nodes (nm):

- 140
- 120
- 100
- 80
- 60
- 40
- 20
- 0

Switch Bandwidth (THz):

- 0.01
- 0.1
- 1
- 10
- 100
Switched Resonators

- Frequency tuning typically done using switched capacitors only
- Tuning range vs Q trade-offs
- Need to switch L’s & C’s for “true” frequency reconfiguration
Requirements for Switching Inductors

• Suppose a PC switch is inserted in series with an inductor $L$ with series resistance $R$ and quality factor $Q_0$.
• In on-state, switch is well represented by $R_{ON}$ if $\omega R_{ON} C_{SW} << 1$ (which is usually true)
• Q-degradation due to reconfiguration is
  \[ \frac{\Delta Q}{Q_0} = \frac{Q_0 - Q'}{Q_0} = \frac{R_{ON}}{R + R_{ON}} \]
• Need $R_{ON} << R$ to prevent significant Q-degradation $\rightarrow R_{ON} < 1 \, \Omega$.
• But $C_{SW} = 1/\omega_{SW} R_{ON}$ is prohibitively large even in nanoscale CMOS and degrades inductor SRF
• Example: Using 32 nm CMOS switch, parasitic resonance of 1 nH inductor @ 15.9 GHz compared to 62 GHz with PC switch
• $R_{ON} < 1 \, \Omega$, $C_{SW} \sim 10$‘s of fF, $R_{OFF} > 10^4$ required to switch L’s.
PC Via-reconfigurable Inductor

\[ Z_{AB,CC} \rightarrow + I_1 \rightarrow R_1 \rightarrow k \rightarrow L_1 \rightarrow L_2 \rightarrow R_2 \rightarrow - I_1 \rightarrow Z_{AB,CC} \]

primary port

Phase-change Chip Fabrication

- Si coated with 10 µm SiO₂
- Sputter 500 nm Cu to form M₁ (underpass)
- Sputter 80 nm SiO₂ and pattern to define via locations
- Sputter 100 nm GeTe and 60 nm TiW to form PC vias
- Sputter 480 nm SiO₂ and lift-off
- Sputter 2 µm Cu to form M₂ (inductor layer)
PC Via-Reconfigurable VCO

Bias switch network

VDD

GeTe switch

GSG probe pads

L2/2

L1/2

VDD

GeTe switch

L2

k

VDD

Cap SW1

Cap SW2

Cap SW3

Cap SW4

Vcont

Bias switch network

VDD

B

Vcont

GeTe switch

GeTe switch
Flip-chip Integration of CMOS and PC chip

Sn solder bumps – connecting signal pins ($V_{out}$’s) and bias pins ($V_{DD}$, GND, $I_{bias}$) between CMOS and carrier PC chips.

PC chip (face up)

CMOS chip (face down)

Flip-chip bond pads

RF probe for testing

GSG1

Single Via Resistance Measurement

- Sub 1 Ω on-resistance
- Off-resistance achieved is lower compared to material properties → due to incomplete amorphization
Transformation Pulse Sequence

- 1st crystallization: 33.6 kΩ
- 1st amorphization: 1 Ω
- 2nd crystallization: 151 Ω
- 2nd amorphization: 31 Ω
- 3rd amorphization: 421 Ω
- 4th amorphization: 18.1 kΩ

- 1st amorphization: 1.53 kΩ
- 2nd crystallization: 151 Ω
- 3rd amorphization: 18.1 kΩ
- 4th amorphization: 31 Ω

- 200 µs
- 2 µs
- 5 ns
- 9.7 V
- 5 ns
- 3.8 V
- 5 ns
- 0.2 V
- 200 µs
Tuning Characteristic and Phase Noise of SC-VCO

![Graph showing tuning characteristic and phase noise of SC-VCO with frequency bands and phase noise levels.]
Phase Noise of SC-VCO

OFF state $f_{OSC} = 3.94$ GHz

ON state $f_{OSC} = 7.08$ GHz
Phase Noise with “Perfect” Vias

- Control experiment
  - On-state → replace PC with metal
  - Off-state → replace PC with oxide
Effect of PC Resistance on Phase-Noise

- Need to transform PC resistances to near material limits to achieve high RF performance
- By transforming to an incompletely crystallized state, on resistance and therefore phase-noise are higher
Cyclability

- Repeatable transformation achieved
- Data is not statistically significant to draw conclusions about reliability
Long-Term Stability

- PC transformed and VCO characterized over several hours
- Stable characteristics over time observed
## Comparison vs Wide-Tuning CMOS VCO’s

<table>
<thead>
<tr>
<th>Ref.</th>
<th>Band (GHz)</th>
<th>TR (%)</th>
<th>ΔF&lt;sub&gt;CENTER&lt;/sub&gt; (GHz)</th>
<th>P&lt;sub&gt;VCO&lt;/sub&gt; (mW)</th>
<th>Phase Noise $\mathcal{L}{\Delta f (Hz)}$ (dBc/Hz)</th>
<th>F&lt;sub&gt;oM&lt;/sub&gt;* (dBc/Hz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Yim, TMTT 2006, 180 nm</td>
<td>0.823-0.867</td>
<td>5.2</td>
<td>0.882</td>
<td>16</td>
<td>-125 @ 600k</td>
<td>-23.6</td>
</tr>
<tr>
<td></td>
<td>1.64-1.814</td>
<td>10.1</td>
<td></td>
<td></td>
<td>-123 @ 600k</td>
<td>-13.62</td>
</tr>
<tr>
<td>Andreani, JSSC 2011 90 nm</td>
<td>2.55-4.08</td>
<td>46.1</td>
<td>2.1</td>
<td>23</td>
<td>-126 @ 1M</td>
<td>2.28</td>
</tr>
<tr>
<td></td>
<td>4.9-5.75</td>
<td>15/9</td>
<td></td>
<td></td>
<td>-125 @ 1M</td>
<td>-2.8</td>
</tr>
<tr>
<td>Kossel, JSSC 2010, 45 nm SOI</td>
<td>7-10</td>
<td>35</td>
<td>3.4</td>
<td>14</td>
<td>-100 @ 1M</td>
<td>-14.7</td>
</tr>
<tr>
<td></td>
<td>9.8-14</td>
<td>35</td>
<td></td>
<td></td>
<td>-97 @ 1M</td>
<td>-12.5</td>
</tr>
<tr>
<td>[Li, JSSC 2005 180 nm]</td>
<td>2.47-2.52</td>
<td>2.0</td>
<td>2.5</td>
<td>4.6</td>
<td>-134 @ 1M</td>
<td>-12.5</td>
</tr>
<tr>
<td></td>
<td>4.95-5.12</td>
<td>3.4</td>
<td></td>
<td>6</td>
<td>-126 @ 1M</td>
<td>-10.9</td>
</tr>
<tr>
<td>Demirkan JSSC 2008 90 nm</td>
<td>10.1-12</td>
<td>17.2</td>
<td>2.2</td>
<td>5.65</td>
<td>-105.5 @ 1M</td>
<td>-10.3</td>
</tr>
<tr>
<td></td>
<td>11.9-14.6</td>
<td>20.1</td>
<td></td>
<td></td>
<td>-103 @ 1M</td>
<td>-9.72</td>
</tr>
<tr>
<td>SC-VCO 130 nm</td>
<td>2.9-4.9</td>
<td>37</td>
<td>2.85</td>
<td>12.5</td>
<td>-107 @ 1M</td>
<td>-12.5</td>
</tr>
<tr>
<td></td>
<td>4.9-7.9</td>
<td>47</td>
<td></td>
<td></td>
<td>-110 @ 1M</td>
<td>-8.25</td>
</tr>
<tr>
<td>CC-VCO 130 nm</td>
<td>4.9-8.5</td>
<td>53.6</td>
<td>1.25</td>
<td>22</td>
<td>-110 @ 1M</td>
<td>-6.1</td>
</tr>
<tr>
<td></td>
<td>5.3-10.6</td>
<td>66.7</td>
<td></td>
<td></td>
<td>-108 @ 1M</td>
<td>-4.8</td>
</tr>
</tbody>
</table>

\[
*F_{oM} = 10 \log \left( \left( \frac{f_{MAX} - f_{MIN}}{\Delta f} \right)^2 \frac{1}{P_{dc}} \right) - \mathcal{L}\{\Delta f\} [8]
\]
PC Switches with Isolated Heater

- Necessary to separate transformation path from signal path for practical application
- Materials and geometries critical to meeting pulse requirements for phase transformation
  - This is the subject of much continuing research

Switch Performance

• Initial measurements indicate good linearity

Future Outlook & Conclusion

• Still in research stage.

• Open questions remain
  – Optimize speed-bandwidth-linearity trade-offs
  – Transformation physics still being understood

• Reliability not conclusively demonstrated

• Phase-change switches demonstrate high promise in reconfigurable radios due to
  – CMOS compatibility
  – Low $R_{ON}$, High $R_{OFF}$
  – Low $C_{OFF}$ $\rightarrow$ very high switch bandwidth
Acknowledgements

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• DARPA RF-FPGA program
• Semiconductor Research Corporation
### PC vs Other Switch Technologies

<table>
<thead>
<tr>
<th></th>
<th>Phase-Change</th>
<th>SiGe</th>
<th>RF-MEMS</th>
<th>GaAs HEMT</th>
<th>P-i-N</th>
</tr>
</thead>
<tbody>
<tr>
<td>$F_{SW} (THz)$</td>
<td>30</td>
<td>0.3</td>
<td>10</td>
<td>0.6</td>
<td>1</td>
</tr>
<tr>
<td>Actuation Voltage (V)</td>
<td>3.3-10 (depends on heater)</td>
<td>1.8-3.3</td>
<td>&gt;10</td>
<td>&lt; 5</td>
<td>&lt;5</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>&gt; 55</td>
<td>30</td>
<td>&gt;60</td>
<td>40</td>
<td>45</td>
</tr>
<tr>
<td>Power Handling (dBm)</td>
<td>&gt; 35</td>
<td>35</td>
<td>35</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>Reliability</td>
<td>?</td>
<td>High</td>
<td>Med-High</td>
<td>High</td>
<td>High</td>
</tr>
</tbody>
</table>