Flipping Bits in Memory Without Accessing Them:

DRAM Disturbance Errors

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Carnegie Mellon  SAFARI  Intel
DRAM Chip

Row
Row
Row
Row
Row
Row
DRAM Chip

Row
Row
Row
Row
Row

Wordline

Opened Row

$V_{HIGH}$
DRAM Chip

Row
Row
Row
Opened Row
Row
Row
Repeatedly opening and closing a row induces **disturbance errors** in adjacent rows.
loop:
    mov (X), %eax
    mov (Y), %ebx
    clflush (X)
    clflush (Y)
    mfence
    jmp loop
loop:
  mov (X), %eax
  mov (Y), %ebx
  clflush (X)
  clflush (Y)
  mfence
  jmp loop

X →

Y →
x86 CPU

```
loop:
mov (X), %eax
mov (Y), %ebx
clflush (X)
clflush (Y)
mfence
jmp loop
```
loop:
  mov (X), %eax
  mov (Y), %ebx
  clflush (X)
  clflush (Y)
  mfence
  jmp loop
Most Modules At Risk

86%  83%  88%
Most Modules At Risk

- After 2010: 86%
- After 2010: 83%
- After 2009: 88%
Most Modules At Risk

After 2010: $10^7$ Errors
After 2010: $10^6$ Errors
After 2009: $10^5$ Errors
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4:30 PM

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