Gather-Scatter DRAM: Improving the Spatial Locality of Strided Access Patterns
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**Observation:** Each row buffer has many useful values
**Idea:** Gather a cache line of useful values in one read

**Column ID-based Data Shuffling**
Goal: Minimize chip conflicts for common patterns
(stage ‘n’ is enabled only if n\textsuperscript{th} least significant bit of column ID is set)

Gather/scatter many access patterns (e.g., any \(2^n\) stride) with near-ideal efficiency and latency!
Minimal support from 1) on-chip caches, 2) instruction set architecture, and 3) software