Estimation of Wafer Cost for Technology Design

W. Maly *, H. Jacobs** and A. Kersch**

Department of Electrical and Computer Engineering*
Carnegie Mellon University
Pittsburgh, Pennsylvania 15213, USA

Siemens AG**
Corporate Research and Development
D-81730 Munich, Germany

Abstract

A simple cost model, capturing relationship between cost of the equipment ownership and the cost of manufacturing wafer, is proposed. This model is constructed in a way allowing for "fair" allocation of the cost of equipment idle time among products fabricated with significantly different technologies, sharing the same fabline. A necessary cost of equipment ownership data base has been built and a number of detailed process flows have been constructed. Finally, cost analysis for three categories of manufacturing scenarios: R&D, ASIC and high volume has been conducted. Results indicate large wafer cost differences between high volume and lower volume manufacturing strategies. These differences also indicate that newer complex processes and manufacturing strategies should be developed with an aid of a cost modeling technique such as one described in this paper.

Introduction

There is a long list of design, manufacturing and process development issues which cannot be properly addressed unless an adequate silicon cost modeling technique is applied. Estimation of true cost gains (or losses) encountered due to introduction of an extra metallization level, allocation of silicon real estate for the self-testing circuitry, estimation of the cost of BiCMOS process, impact of the mismatch between product mix and capacity of the available manufacturing facilities on the wafer cost and many others are among examples of the problems which cannot be solved by using various rules of thumbs or other speculative in nature methods. The purpose of this paper is to address the above cost modeling need, arising in the gap between process operators and design/technology strategists, and to propose a simple wafer cost model. It is also an objective of this paper to provide number of real life cost estimation examples illustrating the feasibility of our approach and highlighting the importance of wafer cost analysis.

Cost Model

Let us assume that the manufacturing floor can be viewed as a set of clusters of individual tools. Each cluster is a group of tools which together perform a processing step. Let us assume also that the manufacturing capacity of the fabline can be characterized by the diagonal matrix $\mathbf{C}_c$ with diagonal elements, $1/c_{cj}$, (for j = 1,2,....,c) which describe the inverse of the capacity for each cluster of tools. The capacity , c_{cj} , is expressed as the number of wafers which can be fabricated at the same time by the j-th cluster of tools. Let the cost of manufacturing of each cluster be characterized by two c -dimensional diagonal matrices: $\mathbf{C}^{\mathbf{a}}$ describing the overall cost (per unit time) of each cluster of tools when it is actively processing wafers and $\mathbf{C}^{\mathbf{i}}$ describing the cost per unit time of each cluster when it is inactive (doing anything but processing wafers). The cost of equipment ownership defined this way should include: cost of equipment depreciation, cost of direct labor, maintenance and materials as well as cost of energy and building depreciation.

Let us also assume that the manufacturing activity on the manufacturing floor is fully characterized by a "cookbook" matrix $\mathbf{R}^0$, where each row of $\mathbf{R}^0$ represents a single process recipe - one row for each product being manufactured. The elements of $\mathbf{R}^0$, t^0_{ij} , (i = 1,2,....., p and j = 1,2,....., s , where p is the number of products and s is the number of steps), describes time which is taken by the product i processed at manufacturing step j . This time includes setup time, waiting time (but not a queuing time), etc. Notice that columns of $\mathbf{R}^0$, representing steps which are performed by the same clusters of tools, can be added and $\mathbf{R}^0$ can be reduced to form a new matrix $\mathbf{R}$. The elements of $\mathbf{R}$, t_{ij} , (i = 1,2,.....,p and j = 1,2,.....,c, where c is the number of clusters) describe cumulative usage of the j-th cluster of tools by the i-th manufactured product.

Finally let the p-dimensional diagonal matrix $\mathbf{V}$, with elements v_j, describes manufactured volume in terms of number of wafers of each product fabricated (or to be fabricated) in a given period of time.

Notice now that columns of matrix **T:**

$$\mathbf{T} = \mathbf{VRC}_c = \begin{bmatrix} \frac{t_{11}v_1}{c_{c1}} & \cdots\cdots & \frac{t_{1c}v_1}{c_{cc}} \\ \vdots & & \vdots \\ \frac{t_{p1}v_p}{c_{c1}} & \cdots\cdots & \frac{t_{pc}v_p}{c_{cc}} \end{bmatrix} \qquad (1)$$

can be used to characterize the total usage of each cluster of tools by time T_j qual to:

$$T_j = \sum_{k=1}^{p} \frac{t_{kj} v_k}{c_{cj}} \qquad (2)$$

Consequently, vector:

$$T = [\, T_1 , T_2, \, ..., \, T_c \,]^T$$

represents usage time of the entire manufacturing floor.

Let us assume now that T^t is the total time of the period being modeled and α_i is a factor determining the time available for production for the i-th cluster of tools. Then vector:

$$\mathbf{T}^{\mathbf{a}} = [\, \alpha_1 T^t , \alpha_2 T^t, \, ..., \, \alpha_c T^t \,]^T \qquad (3)$$

represents the time available for production for the manufacturing floor. Note that matrix $\mathbf{V}$ associated with the T^t period of fabrication must be chosen such that the following inequality is always true:

$$\mathbf{T}^{\mathbf{a}} - T = \begin{bmatrix} \alpha_1 T^t - T_1 \\ \alpha_2 T^t - T_2 \\ \vdots \\ \alpha_c T^t - T_c \end{bmatrix} \geq 0 \qquad (4)$$

Observe also that the total time available on a cluster of machines can be divided into two categories: time when the tools in the cluster are actively processing wafers and time when the tools are inactive (doing anything but processing wafers). The time that the tool is active has already been defined as T_j , where j is a cluster number. The time that the cluster is inactive will be the total time T^t minus the active time, T_j. Furthermore, the inactive time of a cluster can be "allocated" to the products which use that cluster in proportion to the total time usage of the cluster by that product. Hence, the following equation should be true:

$$T^t = \sum_{k=1}^{p} \frac{t_{kj} v_k}{c_{cj}} + \sum_{k=1}^{p} \left[\frac{\frac{t_{kj} v_k}{c_{cj}}}{T_j} \left(T^t - T_j \right) \right] \qquad (5)$$

Let:

$$t^*_{kj} = t_{kj} \frac{T^t - T_j}{T_j} \qquad (6)$$

then for each j Eq. (5) takes the form:

$$T^t = \sum_{k=1}^{p} \left(\frac{t_{kj} v_k}{c_{cj}} + \frac{t^*_{kj} v_k}{c_{cj}} \right) \qquad (7)$$

In other words, the total time for the cluster during the period being modeled can be represented as the sum of the active time each product spends in the cluster and the inactive time "charged" to each product which uses that cluster. Consequently, we can introduce matrix $\mathbf{R}^*$

$$\mathbf{R}^* = \begin{bmatrix} t^*_{11} & .... & t^*_{1c} \\ t^*_{21} & .... & t^*_{2c} \\ \vdots & & \vdots \\ t^*_{p1} & .... & t^*_{pc} \end{bmatrix} \qquad (8)$$

whose elements, t^*_{kj} , are measures of nonproductive times allocated to each product at each manufacturing cluster.

Using the previously defined matrices one can decompose cost of manufacturing into two parts $\mathbf{C}^A$ and $\mathbf{C}^I$ given by the following formulas:

$$\mathbf{C}^{\mathbf{A}} = \mathbf{VRC}_{\mathbf{c}} \mathbf{C}^{\mathbf{a}} \qquad (9)$$

$$\mathbf{C}^{\mathbf{I}} = \mathbf{VR}^* \mathbf{C}_{\mathbf{c}} \mathbf{C}^{\mathbf{i}} \qquad (10)$$

Hence matrix $\mathbf{C}^A$ has the following form:

$$\mathbf{C}^{\mathbf{A}} = \begin{bmatrix} c^a_1 \frac{t_{11} v_1}{c_{c1}} & .... & c^a_c \frac{t_{1c} v_1}{c_{cc}} \\ c^a_1 \frac{t_{21} v_2}{c_{c1}} & .... & c^a_c \frac{t_{2c} v_2}{c_{cc}} \\ \vdots & & \vdots \\ c^a_1 \frac{t_{p1} v_p}{c_{c1}} & .... & c^a_c \frac{t_{pc} v_p}{c_{cc}} \end{bmatrix} \qquad (11)$$

and matrix $\mathbf{C}^I$ can be represented the same way.

Matrices $\mathbf{C}^A$ and $\mathbf{C}^I$ can be directly applied to compute total cost of each product. Simply, by summing two equivalent rows of $\mathbf{C}^A$ and $\mathbf{C}^I$ supplemented with an "overhead term" , C_i^V, (representing costs which do not depend on volume such as costs of lithography masks, design etc.) one can find a portion of a total cost , C_i^T , which should be allocated to the i-th fabricated products using the following expression:

$$C_i^T = C_i^V + \sum_{k=1}^{c} \left(c_k^a \frac{t_{ik} v_i}{c_{ck}} + c_k^i \frac{t_{ik}^* v_i}{c_{ck}} \right) \quad (12)$$

Note that the main feature of the above cost model is an emphasis on the "fair-cost-allocation-policy". In practical terms it means that products which do not use expensive processing steps or "exotic" and infrequently used equipment are not penalized by sharing high costs of these steps.

Implementation

Simple cost modeling strategy described by Equations 1 through 12 can be useful if, and only if, matrices $\mathbf{C^a}$, $\mathbf{C^i}$ and $\mathbf{R}$ are constructed in the way accurately reflecting true cost of equipment ownership and true equipment usage time. In the case of the study reported in this paper these three matrices have been constructed using data and expertise collected from an in-house Siemens cost accounting system. This system has all the capabilities needed to produce cost of ownership data and equipment usage times. To simplify the data extraction process a software interface connecting the cost accounting system with cost modeling software has been built. The cost modeling software itself was implemented in C and was written assuming as input independent variables the product mix (matrix $\mathbf{V}$). It computes cost per wafer of each product using following modification of formula (12):

$$C_i^W = \frac{C_i^V}{v_i} + \sum_{k=1}^{c} \frac{1}{c_{ck}} \left(c_k^a \, t_{ik} + c_k^i \, t_{ik}^* \right) \quad (13)$$

Current software implementation allows also for automatic detection of volume bottle necks [negative elements in vector (4)] and easy modification of the composition of manufacturing floor (matrix $\mathbf{C_c}$).

Wafer Cost Analysis

To study the sensitivity of the cost of the wafer to various attributes of manufacturing process/strategy the following analysis was conducted. First, five processes, all using 6 inch wafers, were chosen (see Table 1) and matrices $\mathbf{R^o}$ and $\mathbf{R}$ for each process were built. In all five cases all processing and metrology operations have been accounted for.

Table 1 . Characteristics of five processes used in the study.

Process (symbol)	CMOS I (PR1)	CMOS II (PR2)	CMOS III (PR3)	Bipolar (PR4)	BiCMOS (PR5)
Number of steps	325	351	407	488	411
Feature s. [µm]	1.5	1.0	0.8	0.8	1.0
Number of metal layers	2	2	3	3	2

Table 2. Characteristics of fifteen manufacturing floors used in the study. "Op. costs" stands for the total cost of operation per year including 20% depreciation in million of German Marks (DM). "Inv. cost" stands for cost of capital investment (equipment) in million of DM. Fabline capacity is expressed in wafer starts per week.

Type of manufact. floor		Floor designed for the process:				
		PR1	PR3	PR1+2+3	PR5	All proc.
"One of each kind"	Symbol	OEK1	OEK3	OEK123	OEK5	OEK12345
	Op. cost	34.8	39.0	47.9	41.1	49.7
	Inv. cost	22.9	26.4	32.4	27.1	30.7
	Capacity	135	89	267	265	295
Minimum fully utilized	Symbol	MFU1	MFU3	MFU123	MFU5	MFU12345
	Op. cost	109.9	117.6	106.7	102.3	125.5
	Inv. cost	68.3	85.8	73.3	68.5	80.0
	Capacity	2k	2k	2k	2k	2k
Custom/ Commod-ity	Symbol	CC1			CC5	
	Op. cost	473.6			295.1	
	Inv. cost	295.1			440.9	
	Capacity	10k			10k	
Custom/ Commod-ity 80/10/10	Symbol			CC123 - 1		
	Op. cost			298.9		
	Inv. cost			464.9		
	Capacity			10k		
Custom/ Commod-ity 10/80/10	Symbol			CC123 - 2		
	Op. cost			248.6		
	Inv. cost			375.8		
	Capacity			10k		
Custom/ Commod-ity 10/10/80	Symbol			CC123 - 3		
	Op. cost			355.3		
	Inv. cost			504.8		
	Capacity			10k		

Then costs of ownership for each piece of equipment required for the five process under investigation were determined (cost data was obtained from actual and current cost database.) Finally fifteen manufacturing floors have been designed. (See Table 2.) Three categories of floors were considered: Low volume (R&D type), medium volume (ASIC type) and high volume type. For low volume fabs it was assumed that they should have a composition minimizing cost of capital investment i.e. they should have "one of each kind" (OEK) of equipment necessary to perform assumed process. Five OEK floors have been designed for the processes: PR1, PR3, PR1 and PR2 and PR3 (assuming equal shares of fab capacity for each process), PR5 and all

five processes combined (also assuming equal share of volumes for each process). These processes have been labeled OEK1, OEK3, OEK123, OEK5 and OEK12345, respectively. For medium size fabs (2k starting wafers per week) the equipment was chosen to maximize utilization level for all major fabrication steps. Five floors - labeled MFU (minimum "fully" utilized) - have been designed for PR1, PR3, PR1+2+3, PR5 and PR1+2+3+4+5 processes, assuming equal volume for all multi-processes floors. Also five high volume (10,000 starting wafers per week) fabs have been designed - two mono-product fabs for processes PR1 and PR5 (labeled CC1 and CC5) and three multi-product fabs for processes PR1, PR2, and PR3. Each of these floors was designed assuming different product mix: (80%, 10%, 10%) , (10%, 80%, 10%) and (10%, 10% 80%) of the volume fabricated with processes PR1, PR2 and PR3, respectively. For each of these fifteen fabs cost of capital investment and cost of operation have been computed. Of course, for each floor matrices $\mathbf{C^a}$, $\mathbf{C^i}$ and $\mathbf{C_c}$ have been constructed as well.

In the final stage of investigation reported in this paper the cost modeling software, described in previous section, was used to compute cost per wafer assuming $C^v{}_i = 0$. The results are shown in Tables 3 and 4.

Table 3. Cost per wafer for low and medium volume fablines.

Type of manu. floor	Processes:				
	PR1	PR3	PR1+2+3	PR5	PR1+2+3+4+5
OEK1	3388				
OEK3		5941			
OEK123			2201,2133,2953		
OEK5				2047	
OEK12345					2137,1686,2443,3043,2468
MFU1	682				
MFU3		857			
MFU123			702,565,828		
MFU5				685	
MFU12345					681,546,911,1129,731

Table 4 . Cost per wafer for high volume fablines.

Manufact. floor	Process:		
	PR1+2+3 80/10/10	PR1+2+3 10/80/10	PR1+2+3 10/80/10
CC123 - 1	587,475,805 (8k, 1k, 1k)		
CC123 - 2		622,445,788 (1k, 8k, 1k)	
CC123 - 3			639,472,749 (1k, 1k, 8k)

Discussion of the Results

Data presented in Tabs. 3 and 4 may be analyzed from various standpoints. Here we list the following observations which, in our opinion, should be highlighted:

1. Wafer cost is a strong function of manufacturing volume. This obvious observation is strongly emphasized by the data in Tables 3 and 4 which show that cost per wafer in R&D setting can be up to 7 times higher than the cost of the wafer fabricated in the high volume fabs. (Compare the cost of the wafer produced in OEK3 fab with PR3 process and wafer produced with the same process in CC123-3 fab.)

2. Wafer cost is a function of the product mix (See data in Table 4).

3. Cost of BiCMOS process is much higher than it could be anticipated based on the number of steps only. (Compare process PR2 and PR5. PR5 has 17% more steps but is around 34% more expensive. See cost of the wafers for process mixes PR1+2+3+4+5 shown in Table 3.)

4. Cost increase which is due to the decrease of the minimum feature size is higher than was expected. For example by comparing processes PR2 and PR3 run on CC123 floor one can find that 0.8 µm process is 1.79 times more costly than 1µm process.

Conclusions

The purpose of this paper was to propose a cost modeling technique and to provide number of real life cost estimation examples highlighting the importance of wafer cost analysis. Such model was proposed and obtained results indicate large wafer cost differences among various manufacturing strategies. These differences also indicate that newer complex processes and manufacturing strategies should be developed with an aide of a cost modeling technique such as one described in this paper.

Acknowledgments

Authors would like to thank Anne Gattiker and P.K. Nag from Carnegie Mellon University for the help with development and implementation of the cost model as well as Mr. Ehm and his colleagues of the Integrated Submicron Silicon Technology Center (ISTC), Siemens Semiconductor Division, for the assistance with the cost data collection. Also we would like to express our gratitude to Dr. Armin Wieder, Director, Application Center Microelectronics, Siemens Corporate R&D, for the sponsorship and vision which made our task possible.