Timing Recovery for Data Storage Systems

Prof. Vijayakumar Bhagavatula
Data Storage Systems Center (DSSC)
Carnegie Mellon University, Pittsburgh, USA

As magnetic recording track densities increase, signal-to-noise ratio (SNR) will decrease and as linear density increases, inter-symbol interference (ISI) will increase. One of the approaches being investigated for dealing with increased ISI and decreased SNR is based on iterative soft decoding (e.g., turbo codes and LDPC codes). However, the expected coding gains assume that the timing recovery is working perfectly. An important component of current timing recovery systems is a simple data detector, which will produce errors in low SNR and high ISI leading to degraded timing recovery performance and possibly *loss of lock* (loss of lock refers to the event where the estimated timing differs significantly from the actual timing for a long interval causing a failure of error correction codes). When loss of lock happens, the rest of that data block (until the next acquisition region) is unreliable. Also, the loop latency needs to be small to keep the timing recovery loop stable. Another phenomenon of concern in magnetic tape recording systems is *dropouts*, during which readback pulse amplitudes, widths and positions may change from the nominal values. Our research is aimed at investigating the fundamental relationships between the relevant parameters (e.g., SNR, normalized density, dropout distributions, distributions of phase and frequency offsets, and loop latency) and timing recovery performance limits. This will help us in determining the gaps between the performance of candidate timing recovery architectures (e.g., phase-locked loop (PLL), interpolation timing recovery (ITR) and Kalman filter (KF)) and theoretical limits and to determine the directions for future enhancements. Our recent research contributions in the area of advanced timing recovery for data storage channels include:

- We developed a timing recovery simulator that allows the introduction of different timing disturbances and used it to numerically investigate the acquisition and tracking performances [1].
- We investigated the use of bit-flipping to achieve run length constraints in LDPC-coded channels [2, 3].
- We developed an implementation-friendly equalizer adaptation method that decouples the equalizer adaptation from AGC and timing recovery loops.
- We developed the Cramer-Rao lower bound for phase estimation with various preamble patterns [4].
- We developed a closed form expression for Kalman filter's mean squared error under imprecise priors [5] in order to quantify the robustness of the KF approach to assumptions about parameters.

Towards the goal of developing advanced timing recovery methods for low-SNR and high-ISI data storage systems, we are investigating the use of **Kalman filtering** methods for various tasks in timing recovery including: acquisition, zero phase start and tracking. In the decision–directed timing recovery loop, a Viterbi detector (VD) is usually used to estimate bit decisions to be used in timing error detector (TED). The VD and the TED both introduce loop delay. In low-SNR and high-ISI channels, a longer delay in VD may be necessary in order to obtain sufficiently reliable decisions as inputs to the TED. However, longer **loop delay** degrades the dynamics of the phase-locked loop (PLL) and results in larger timing jitter and smaller stability margin. We are investigating methods [6, 7] to compensate for the loop delay. The goal of the acquisition stage is to estimate the initial phase and frequency offsets. The conventional timing acquisition uses a zero phase start (ZPS) followed by a phase-locked loop (PLL) with fixed loop gains (α for phase update gain and β for frequency update gain). After successful acquisition, the tracking stage may begin with smaller fixed loop gains. Simulation suggests this approach works well for small frequency offsets (up to 1%), but does not work if the frequency drift is larger. We are developing a Kalman filter (KF) based method for **acquisition in large frequency offset**.

[1] J. Liu, H. Song, and B.V.K. Vijaya Kumar, "Timing acquisition for low-SNR data storage channels," *IEEE Trans. Magn.*, Vol. 39, Issue 5, 2558-2560, 2003.
[2] Zongwang Li, J.Xie and B.V.K. Vijaya Kumar, "An improved bit-flipping scheme to achieve run length control in coded systems," *IEEE Trans. Magnetics*, Vol. 41, 2980-82, 2005.
[3] Zongwang Li and B.V.K. Vijaya Kumar, "Low-density parity check codes with run length limited (RLL) constraints," *IEEE Trans. Magnetics*, Vol. 42, 344-349, 2006.

[4] J. Xie, Zongwang Li and B.V.K. Vijaya Kumar, “Maximum likelihood estimation of phase from preambles with harmonics,” *ISOM/ODS Technical Digest*, 2005.
[5] J. Xie, L. Sun and B.V.K. Vijaya Kumar, “Analysis of Kalman Filter in timing acquisition in data storage read channels,” *Proc. GlobeCom*, 2364-2368, 2005.
[6] A. Patapoutian, “Application of Kalman filters with a loop delay in synchronization,” *IEEE Trans. Commun.*, Vol. 50, May 2002.
[7] J. Xie and B.V.K. Vijaya Kumar, “Timing recovery loop delay compensation by lowering loop gains,” *ICC 2006*, Istanbul, Turkey, June 2006.