DSSC Research in Data Storage Channels

Vijayakumar Bhagavatula
- Structured low density parity check (LDPC) codes
- FPGA-based LDPC code evaluations
- Modulation constraints + LDPC codes
- Timing recovery for low SNR channels
LDPC Codes

\[
\begin{bmatrix}
    s_0 \\
    s_1 \\
    s_2 \\
    s_3
\end{bmatrix} =
\begin{bmatrix}
    1 & 0 & 0 & 0 & 0 & 1 \\
    0 & 1 & 0 & 1 & 1 & 0 \\
    0 & 0 & 1 & 1 & 0 & 0 \\
    0 & 0 & 0 & 1 & 1 & 0
\end{bmatrix}
\begin{bmatrix}
    \hat{x}_0 \\
    \hat{x}_1 \\
    \hat{x}_2 \\
    \hat{x}_3 \\
    \hat{x}_4 \\
    \hat{x}_5
\end{bmatrix}
\]

\[x\text{ is valid codeword if } s = Hx = 0\]
LDPC Decoding

Soft Information

Check to bit update

Bit-to-Check update
- Soft detection and decoding
- Exchanging soft information between channel detector and LDPC decoder
- 3~5 dB Gain over uncoded PRML system at BER $10^{-5}$
A set \( \{a_1, a_2, \ldots, a_j\} \) of different residues (mod \( v \)) is called a difference set \((v, j)\) if no two of the ordered \( j(j-1) \) differences \( a_i - a_i' \) modulo \( v \) are identical.

Assume \( D_1, D_2, \ldots, D_t \) are disjoint difference sets \((v, j, t)\), we can construct 4-cycle-free DDS-LDPC code \((N = vt, j, k = jt)\) with \( H = [H_1 \ H_2 \ \cdots \ H_t] \).

DDS-LDPC codes with column weight \( j \geq 3 \) have girth \( g = 6 \).

DDS-LDPC codes have minimum distance \( j + 1 \leq d_{\text{min}} \leq 2j \).
Array LDPC codes

\[ H = \begin{bmatrix}
I & I & I & \ldots & \ldots & \ldots & I \\
I & \partial & \partial^2 & \ldots & \ldots & \ldots & \partial^{k-1} \\
\ldots & \ldots & \ldots & \ldots & \ldots & \ldots & \ldots \\
I & \partial^{j-1} & \partial^j & \ldots & \ldots & \ldots & \partial^{(k-1)(j-1)} \\
\end{bmatrix} \]

\[ I = \begin{bmatrix}
1 & 0 & \ldots & 0 & 0 \\
0 & 1 & \ldots & 0 & 0 \\
\ldots & \ldots & \ldots & \ldots & \ldots \\
0 & 0 & \ldots & 0 & 1
\end{bmatrix}_{p \times p}, \quad \partial = \begin{bmatrix}
0 & 0 & \ldots & 0 & 1 \\
1 & 0 & \ldots & 0 & 0 \\
\ldots & \ldots & \ldots & \ldots & \ldots \\
0 & 0 & \ldots & 1 & 0
\end{bmatrix}_{p \times p} \]
Each $H_{ij}$ is either an all-zero matrix or a circulant matrix.

Quasi cyclic LDPC code (QC LDPC) with parity check matrix in circulant form is a good candidate for data storage systems:

- **Low error floor (compared to Turbo codes)**
- **Hardware friendly architecture**
- **Low routing congestion in ASIC** (regular structure of $H$ matrix)
- **Low complexity decoding**
- **Good girth**
Comparison of Hardware Platform for DSP Algorithm

**uP**: General Purpose Microprocessor / Digital Signal Processor

**ASIC**: Application Specific Integrated Circuit

- **FPGA**
  - EPR4 target, depth=15, two-step SOVA
  - Operations/bit ~200.
  - Assume 1GHz PC, 3 clock cycles/operation. $10^{13}$ bits need 69 days
  - 100Mbps, $10^{13}$ bits need 1.15 days

- **uP**
  - Assume 1GHz PC, 3 clock cycles/operation. $10^{13}$ bits need 69 days
  - 100Mbps, $10^{13}$ bits need 1.15 days

**Matlab, C**

**PCI Port**

**Xilinx FPGA**

**FPGA board**
Hardware / Software Co-design

**Task Partition:**

- **Generate Samples**
  - PC
  - PCI Port

- **Collect Errors**
  - PC
  - PCI Port

- **Detection/Decoding**
  - FPGA

- **High speed sample generation**
- **High bandwidth**

Carnegie Mellon
FPGA Platform for PR channel

- Start, stop, noise variance, max error
- PCI (33.33 MHz) handshaking
- Error Location, Error number, Error distribution

- Reconfigurable block size, column weight, bit width, iteration number
- Suitable for a broad class of LDPC codes
- High throughput: for (4617, rate 8/9) code in AWGN, 2Gbps/iteration at 100MHz
DDS J=3 Code Performance

DDS J=3, N=4923, M=547

AWGN Channel Result at 50 LDPC iteration

PR channel with 25 LDPC iterations and 2 channel iterations

C Simulation

BER

BLER

SNR

10^{-8}
DDS J=5 Code Performance

DDS J=5, N=4923, M=547

BER/BLER

AWGN Channel at 50 LDPC iteration

PR Channel with 25 LDPC iterations and 2 channel iterations
Array Code $J=3$ Performance

ARRAY $j=3$, $N=4671$, $M=519$

BER

BLER

AWGN Channel Result at 50 LDPC iteration

PR channel with 25 LDPC iterations and 2 channel iterations
Array Code Performance in AWGN

Possible Due to FPGA

7 days@100MHz
Rate 8/9 QC-LDPC Code

Code length: 5760
Message length: 5120
Code rate: 8/9

Column Weight: 3, 4, 5
Row weight: 27,36,45

Max. # iterations: 15
Encoding:

Input Sequence:

1110001010011011110001110010001110101
001101001001010100101010101010100011

Column Parity

Row Parity

111000101001
101111000110
010001110101
001101001001
010010101010
101010100011

0
1
0
1
1
0

0
1
0
1
1
0

Turbo Product Code/Single Parity Check (TPC/SPC) Code
Decoding

\[
\begin{array}{cccccccccccc}
1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 1 \\
1 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 0 \\
0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 0 \\
0 & 0 & 1 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 \\
0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\
1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 1 \\
\end{array}
\]

Row Parity

\[
\begin{array}{cccccccccccc}
1 & 1 & 1 & 0 & 0 & 0 & 1 & 0 & 1 & 0 & 0 & 1 \\
1 & 0 & 1 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 0 \\
0 & 1 & 0 & 0 & 0 & 1 & 1 & 0 & 1 & 0 & 1 & 0 \\
0 & 0 & 1 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 0 & 1 \\
0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\
1 & 0 & 1 & 0 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & 1 \\
1 & 1 & 0 & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 1 & 0 \\
\end{array}
\]

Column Parity

Exchange Information
Each TPC/SPC codeword contains 960 bits (32x30), of which 61 bits are parity bits
A sector contains 5 TPC/SPC codewords, i.e., 305 parity bits (about 30 10-bit RS code symbols).
Thus, TPC/SPC beneficial only if it offers at least 15 fewer symbol errors than without it.
Calculate the error symbols using direct count
  - after soft output Viterbi algorithm (SOVA)
  - after TPC/SPC decoder
- 1665626 symbol errors at 7dB
- 49344 symbol errors at 8dB
- 1937 symbol errors at 9dB

- TPC has 305 parity bits.
- For coding gain: The gap between SOVA and TPC output >15 symbols
- Transition noise
  - Transition jitter noise
  - Transition width variation
- Media nonlinearities
  - Nonlinear transition shift (NLTS)
  - Partial erasure (PE)
- Inter-symbol interference
- Electronic Noise
A single pulse

PW50 is the pulse width at 50% of the peak amplitude

$E_t$ is the single pulse energy

Readback signal

Binary information written as $a_k = +1$ or -1.

$b_k$ is the difference of $a_k$:

$$b_k = a_k - a_{k-1}$$
The jitter noise will cause a random shift in transition position (or a reading timing error)

\[ y(t) = \sum_k b_k h_k (t - kT + \delta_k) \]

\( \delta_k \) is a Gaussian random variable representing the transition jitter.

\( h_k \) is time varying (PW50 is a Gaussian variable)

Partial Erasure (PE)
- Each bit cell is partially erased by the field of neighboring field (when transition occurs)
- Results in an amplitude loss in the readback signal

Nonlinear Transition Shift (NLTS)
- The previous written bit cells interfere with the current writing field
- Results in a transition shift

\[ y(t) = \sum_{k} f_k b_k h_k \left( t - kT + \delta_k - \frac{\varepsilon T}{4} b_k b_{k-1} \right) \]

- \( f_k \) is the effective PE ratio:
  - \( f_k = 1 \) if no transition occurs in adjacent boundaries
  - \( f_k = \gamma \) if one transition
  - \( f_k = \gamma^2 \) if two transition
  - \( \gamma \) is the partial erasure ratio, \( \gamma < 1 \)

\( \varepsilon \) is the NLTS factor. Note that NLTS effect happened only when consecutive transitions appear.
The goal is to evaluate codes under more realistic signal impairments
The overall system (LDPC encoder/decoder, SOVA and the recording channel) is implemented on a Xilinx Virtex II 8000 FPGA device
EPR4 equalizer is a 11-coefficient FIR filter
- $E_t$ single pulse energy
- $N_0$ height of the additive white noise power spectral density

The modified channel model

\[ h^j(t) = \frac{\partial h(t, w)}{\partial t}, \quad h^w(t) = \frac{\partial h(t, w)}{\partial w} \]

\[ SNR = \frac{E_t / N_0}{1 + 4 \frac{\sigma_j^2 + \sigma_w^2}{PW 50^2} \frac{E_t}{N_0}} \]

$\sigma_j$ and $\sigma_w$ are the standard deviations of jitter noise and width variation.

Overall Simulator Structure

Flowchart:
- RDG → ENC → Interleaver
- Magnetic Recording Channel
- SOVA → Deinterleaver
- ERR ANY
- Write processor
- Read processor
### Simulator Settings

<table>
<thead>
<tr>
<th>FPGA Chip</th>
<th>Xilinx Virtex II 8000</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Adaptor</strong></td>
<td>AlphaData ADM-XRC-II PCI Adaptor</td>
</tr>
<tr>
<td><strong>Hardware Programming</strong></td>
<td>VHDL</td>
</tr>
<tr>
<td><strong>language</strong></td>
<td></td>
</tr>
<tr>
<td><strong>LDPC Code</strong></td>
<td>Code length 4932, rate 8/9</td>
</tr>
<tr>
<td><strong>Column Weight</strong></td>
<td>$j = 3$</td>
</tr>
<tr>
<td><strong>PR target</strong></td>
<td>EPR4</td>
</tr>
<tr>
<td><strong>SNR region</strong></td>
<td>12dB --- 22 dB</td>
</tr>
<tr>
<td><strong># of iterations</strong></td>
<td>25 LDPC iterations</td>
</tr>
<tr>
<td></td>
<td>2 channel iterations</td>
</tr>
</tbody>
</table>
The resource utilization (Xilinx Virtex II 8000 -4)

- Total equivalent gate count for design: 3,696,944

<table>
<thead>
<tr>
<th>Number of Slices</th>
<th>Number of Slice Flip Flops</th>
<th>Number of 4 input LUTs</th>
<th>Number of MULT18X18s</th>
<th>Number of GCLKs</th>
</tr>
</thead>
<tbody>
<tr>
<td>17897 out of 46592 38%</td>
<td>15936 out of 93184 17%</td>
<td>27308 out of 93184 29%</td>
<td>56 out of 168 33%</td>
<td>1 out of 16 6%</td>
</tr>
</tbody>
</table>

Processing speed and throughput

- Clock speed 40 Mbits/s
- Throughput 180 Mbits/s per iteration
- Actual throughput (simulation) 37 Mb/s
- Time required to reach BER of 10^{-11}: FPGA ~ 30 hours
  - C simulation  >3,000 hours
High Electronic Noise (Electronic Noise: Transition Noise = 9:1)
Normalized Density = 1.0

Bit Error Rate

Frame Error Rate
Medium Transition Noise (1:1)
Normalized Recording density = 1.0

Bit Error Rate

Frame Error Rate
High Transition Noise (1:4)  

Normalized Recording Density: 1

Bit Error Rate  
Frame Error Rate
BER reaches $10^{-8}$ for transition noise to electronic noise ratios of 1:9, 1:1, and 4:1 at 18.5, 18, 16 dB respectively.

The SOVA-LDPC code system appears to be more robust to transition noise than to AWGN.

Error floor appears in all 3 cases.

Error floor starts at around BER of $10^{-8}$ for the rate 8/9 column weight 3 LDPC code.
At normalized recording density of 2, the BER reaches $10^{-8}$ at the SNR level of 17.5
- BER and FER performance without media nonlinearities (PE & NLTS)
Effect of Media Nonlinearities

- Comparison of BER and FER between systems with and without media nonlinearities

- At normalized recording density of 2, the system suffers about 3.2 dB loss due to media nonlinearities
Effect of Partial Erasure

- BER and FER performance for different PE ratios at SNR of 15.5 dB (no NLTS)

- The PE effect will decrease the signal level for consecutive transitions
- When PE ratio decreases to 0.7, the performance loss is significant
Effect of NLTS

- BER and FER performance for different NLTS levels at SNR of 15.5 dB (no PE effect)

- The NLTS effect will alter the transition position
- When NLTS level reaches 15% of bit length, the performance loss is significant
The performance degradation from density 2 is more than 6 dB
EPR4 target is not effective for density 2.6
Comparing the bit errors eliminated as the iterations progress, the first 10 iterations and the channel iteration are the most efficient.

All iterations contribute in the waterfall region.

In the error floor region, the iterations are less effective after 10 iterations.
With Fewer Iterations

- Reduce the total number of iterations to 10 (in 2 channel iterations) from 50
- The loss in BER is 1.1 dB in the waterfall region
- The difference is smaller in the error floor region
- The guaranteed throughput is increased by 5
LDPC and other coding schemes can offer excellent error correction capabilities.

LDPC decoders need soft information as input whereas standard RLL decoders output hard bits.

Vasic and Pedagani proposed introducing deliberate bit errors (bit flipping) to satisfy Run-Length-Limited (RLL) constraints (TransMag, 1738-1743, May 2004) that the LDPC decoders may be able to correct.

Above scheme does not work well if the number of deliberately introduced bit errors is large.

We propose a modification to reduce the # of bit flips.
Improved via a linear feedback shift register (LFSR)
Soft Iterative Detection

Initial value from header field (or be protected by a short block code)

Receive sequence

SOVA/BCJR channel detector

Separator

Sign bits

LFSR

LDPC Decoder

Decoded user bits

Reliability value

XOR’ed sign bits

Reliability value
Low-frequency Content
BER of LDPC+RLL

![Graph showing BER of LDPC with VR2 and DC free constraint, LDPC with VR2 and DC free constraint, LDPC with VR2 and DC free constraint, and LDPC no flip. The x-axis represents Eb/N0 (dB) and the y-axis represents BER. The graph compares the performance of different LDPC configurations at various Eb/N0 values.](image-url)
Timing Recovery

\[ y(t) = \sum_{k=-\infty}^{\infty} a_k h[t - kT - \tau(t)] + n(t) \]

- \( a_k \) the channel bit (i.e., the bits after the modulation code encoder) sequence
- \( h[t-\tau(t)] \) the time-varying channel pulse response showing explicitly the effect of the phase drift

- Timing recovery estimates \( \tau(t) \) so that synchronous samples (i.e., samples of \( y(t) \) corresponding to \( t = kT \) if \( \tau(t) \) were zero) can be extracted for further processing by channel detector
- Future storage channels will employ advanced coding and detectors that can cope with very low SNRs, but timing recovery methods may not be able to handle such low SNRs
Timing Recovery: Current Approach

Format for Sectors

- **Preamble**
- **Synch Mark**
- **User Data**

**Acquisition Mode**

**Tracking Mode**

Diagram showing the flow of signals and components involved in timing recovery.
The event where the recovered clock differs significantly from the actual clock for a significantly long duration leading to error bursts, that may be uncorrectable by the ECC and thus destroy entire sectors of data.
Kalman-filter based Timing Recovery

Table of Pre-calculated PUG value of Each Bit for First Filter

Table of Pre-calculated FUG value of Each Bit for First Filter

Table of Pre-calculated PUG value of Each Bit for Second Filter

Table of Pre-calculated FUG value of Each Bit for Second Filter

Timing Error Detector (TED)

Simple Data Detector

Decision

2 to 1 Selector

Equalizer

VCO

PR

D

PR is phase register
FR is frequency register

FR is frequency register

Continuous Signal

VCO is digitally controlled
Converts amplitude to time

Patent Pending

Dual Segmented Kalman filter-based Storage Timing Recovery (DSK-STR)
Loss of Lock Rates

Conventional Hard Decision Directed TED Scheme
SDD-TED DSK-STR
Hard Decision Directed DSK-STR
SDD-TED DSK-STR Linear Phase Drift Model
SDD-TED Single Segmented-Kalman-Filter

SNR (dB)

Loss of Lock Rate

SNR (dB)

10^{-5} 10^{-4} 10^{-3} 10^{-2} 10^{-1}
Summary

- New implementation-friendly structured LDPC codes being designed and evaluated
- LDPC codes with runlength and DC control
- FPGA Platform enabling us to investigate code performance at very low BERs & error floors
- Enhancing the FPGA platform to include more realistic signal impairments
- New methods for timing recovery in low SNR