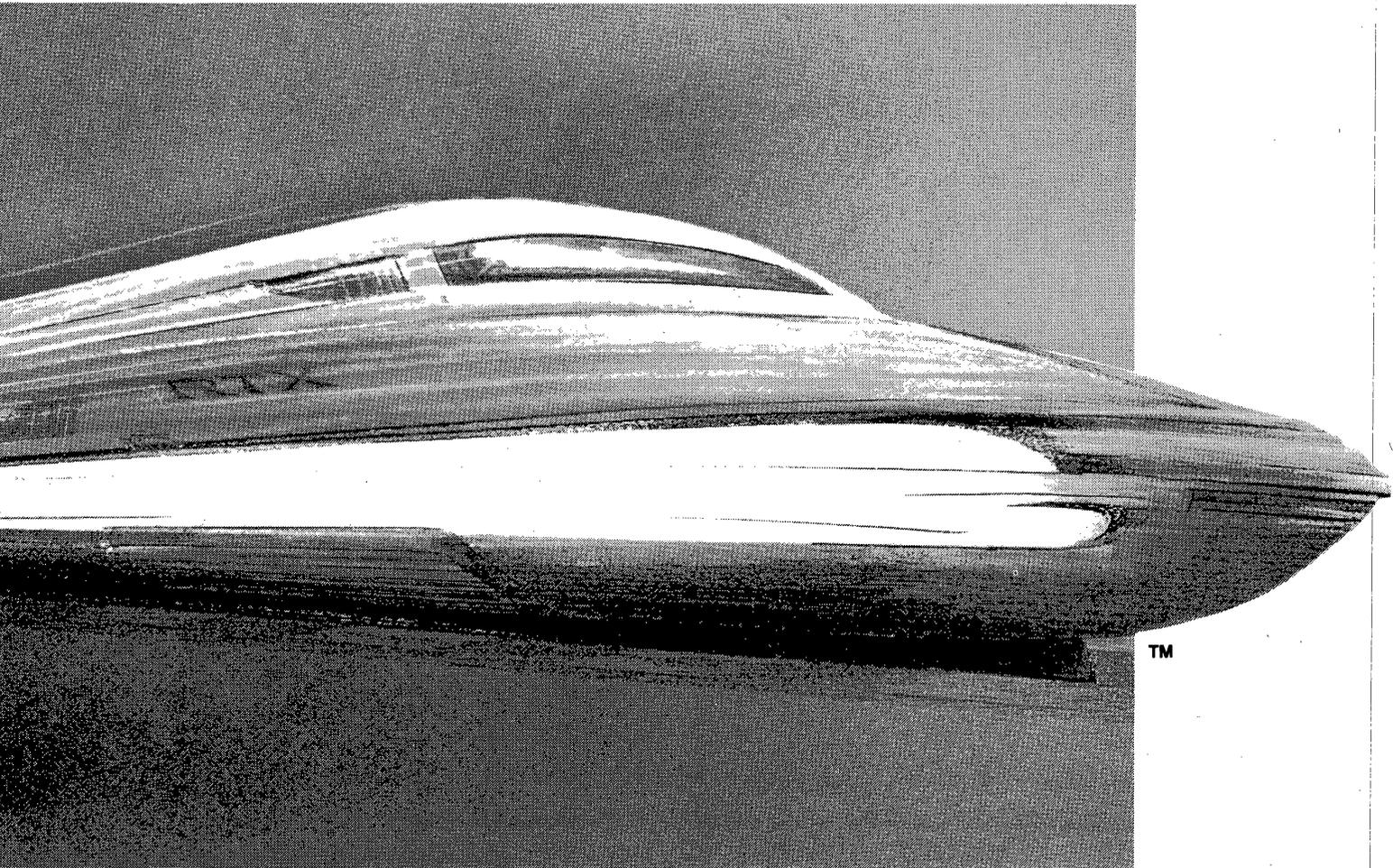


RTXX™

*R e a l T i m e E x p r e s s*



1989 SEMINAR PRESENTATION

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# RTX SEMINAR

## Real Time Express

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For more information please call: (407) 724-7302  
Harris Semiconductor  
RTX™ Marketing  
MS 62A-021  
P.O. Box 883  
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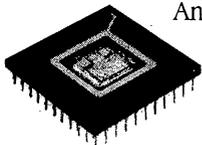


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# First You Dress Like An Engineer...



## ...Then You Climb Aboard The Real Time Express.™



And leave behind all the performance limitations of traditional microprocessors.

Harris' Real Time Express™ offers you micro-controller integration and RISC processor speed — 15 MIPS (typical) at 10 MHz — all for a fraction of the power dissipation of conventional designs.

The RTX 2000™ is the first in a family of general purpose, application-specific and semicustom products addressing your real-time performance requirements:

- Rapid interrupt response • Predictable timing
- Fast context switching • Hardware extensibility (via ASIC Bus™) • No need for costly in-circuit emulators

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- Dual-stack Quad Bus™ architecture which eliminates caches and pipelines • Programming in a structured high-level language (C, Forth, Prolog) • Interactive debugging — at full speed — with full symbolic support

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**In U.S.: 1-800-4-HARRIS Ext. 1288 (literature), or Ext. 1299 (seminars).**

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### Train Adventure Giveaway! Details at Seminar

EDN101388

- Send me a seminar schedule and save me a free engineer's cap
- Tell me more about RTX™; send technical literature.
- Let's talk...Have an RTX™ specialist contact me soon.

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# RTX SEMINAR



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REAL TIME EXPRESS™

A NEW CONCEPT  
FOR REAL-TIME CONTROL

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# RTX SEMINAR



## SEMINAR OBJECTIVES

- Explore the Challenges Associated with Designing Real-Time Control Systems
- Examine Programming Languages Which Address the Needs of Real-Time Systems
- Discuss Development System Environments and Their Impact on Productivity
- Look at Various Hardware/Software Solutions for Real-Time Systems
- Provide Information on the Harris RTX Solution

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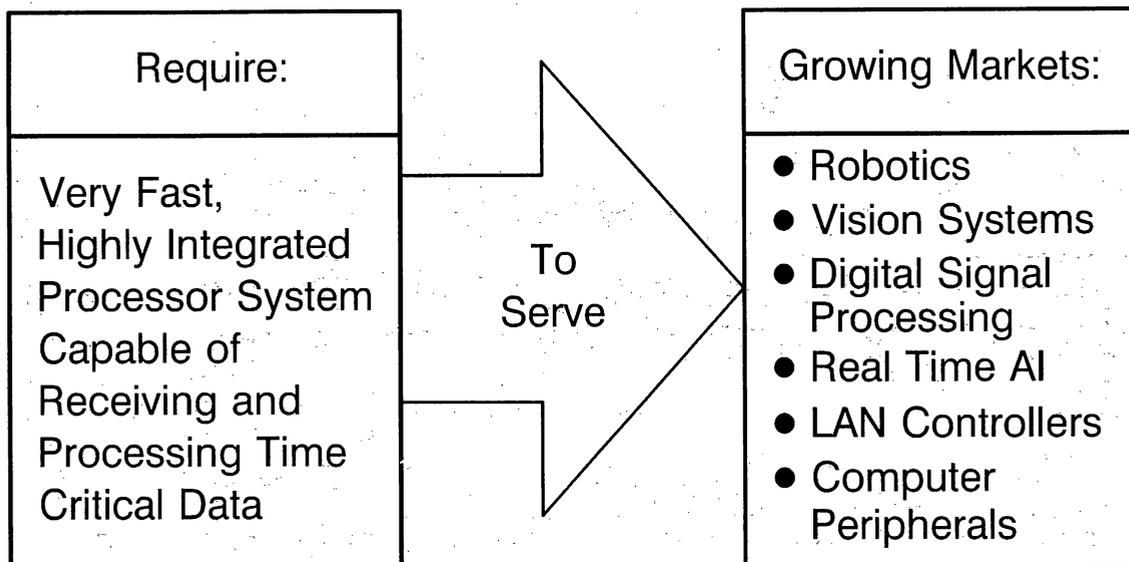
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# RTX SEMINAR



## REAL-TIME CONTROL SYSTEMS



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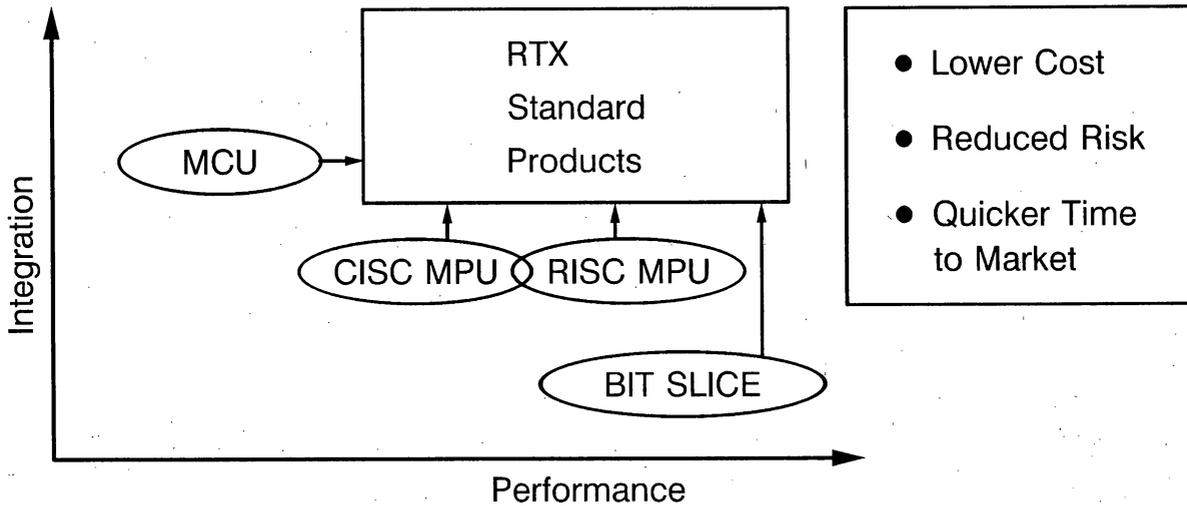


# RTX SEMINAR



STANDARD PRODUCT ALTERNATIVE TO CUSTOM

## HIGH SPEED/HIGH INTEGRATION



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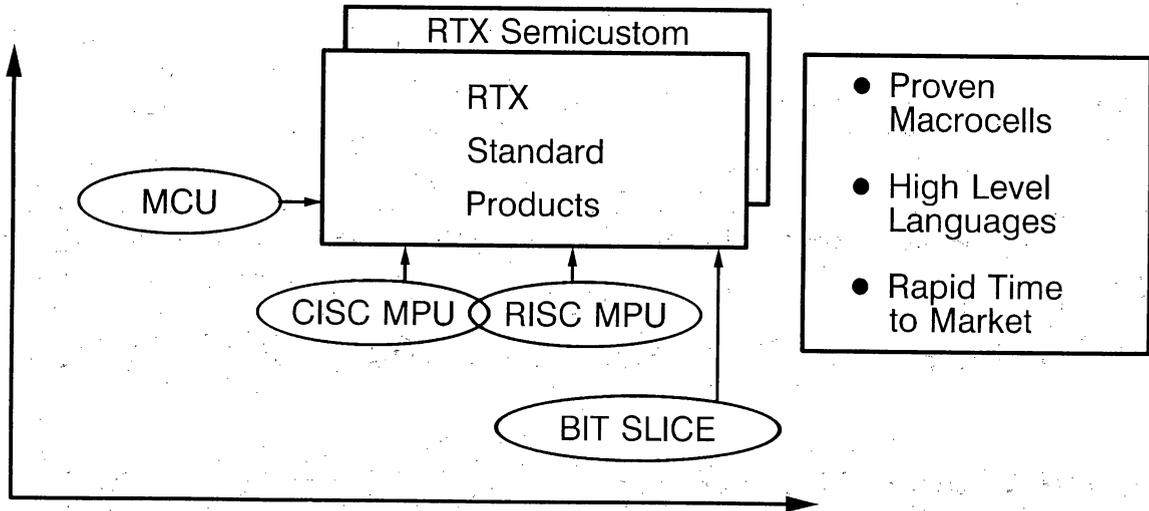


# RTX SEMINAR



## SEMICUSTOM EXTENSION

### FURTHER SPEED, INTEGRATION ENHANCEMENT



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# RTX SEMINAR



REAL TIME EXPRESS

## CHALLENGES ASSOCIATED WITH THE DESIGN OF REAL-TIME CONTROL SYSTEMS

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# RTX SEMINAR



## FAST RESPONSE TO REAL-TIME EVENTS

- Interrupt Driven Systems Must Service the Request Quickly
- Multitasking Controller Applications Require Fast Context Switch
- In Real-Time Systems,  
“A Late Answer Is a Wrong Answer”

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# RTX SEMINAR



## PREDICTABILITY

- Caches and Pipelines Create Uncertainties in Interrupt Response Time and Speed of Execution
- “Stochastic” System Designs Complicate Testing and Debugging
- Predictable, “Deterministic” Systems Reduce Designers Headaches

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# RTX SEMINAR



## LOW POWER REQUIREMENTS DESIRABLE

- Harsh Environments May Dictate Sealed Enclosures with No Convection Cooling
- High Density Packaging Prohibits Use of Power Hungry Components
- Battery Operation and Power Fail Backup Often Desirable
- "Sleep Mode" Provided by Static Designs Useful in Many Applications
- Lower Temperatures Enhance System Reliability

0189-011



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## SPECIAL MEMORY REQUIREMENTS

- Embedded Systems May Have Physical Size Limitations
- Unlike General Purpose Workstations, Embedded Systems Often Do Not Require Large Memory Arrays and Associated Overhead
- System Should Permit Selective Use of Fast Memories
- Compact Code Minimizes Memory Usage and Allows More Expansion Space

0189-012



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## TIME TO MARKET

- Complex Systems Require Lengthy Learning Curves for Designers
- Cost Estimates, Project Schedules, and Proposals Are Troublesome, Inaccurate, and Time Consuming for Complex System Designs
- Competitors with Simple, Efficient Solutions Are a Threat to Your Market Opportunity

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# RTX SEMINAR



REAL TIME EXPRESS

WHY IS IT DIFFICULT  
TO DEVELOP SOFTWARE  
FOR EMBEDDED  
REAL-TIME SYSTEMS?

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# RTX SEMINAR



## TESTING OF EMBEDDED SYSTEMS

- Simultaneous Debugging of Unproven Hardware *and* Software
- Programmer Has Little Visibility Into System Under Test
- Responses of an Embedded System Often Reflect Second or Third Level Effects

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# RTX SEMINAR



## HIGH LEVEL LANGUAGES TYPICALLY AREN'T FAST ENOUGH

- Optimizing Compilers Make Unpredictable Trade-Offs Between Execution Speed and Code Size
- Many Languages Don't Support Real-Time Features
- Critical Sections Still Must Be Done in Assembly Language

0189-020



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# RTX SEMINAR



REAL TIME EXPRESS

## RTX 2000 SOLUTION TO EMBEDDED REAL-TIME CONTROL SYSTEMS

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# RTX SEMINAR



## RTX 2000 ARCHITECTURE OVERVIEW

- Simplicity - Predictable Operation, No Pipeline
- RISC-Like - Hardwired Instruction Decode
- Parallelism - Quadbus, Four Independent Busses
- Stack Based - High Speed On-Chip Stacks
- Addresses 1 Megabyte of Memory
- Flexible Hardware - Software Partitioning
- Extensible Architecture - ASIC Bus

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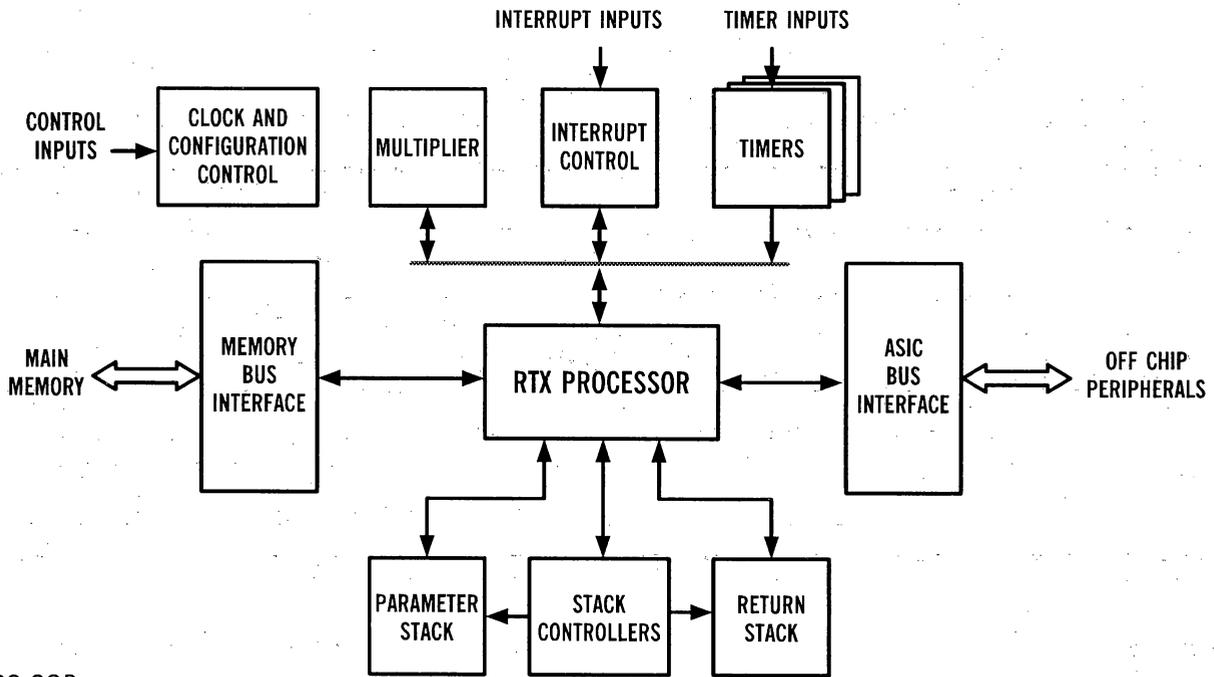
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# RTX SEMINAR



## RTX 2000 BLOCK DIAGRAM



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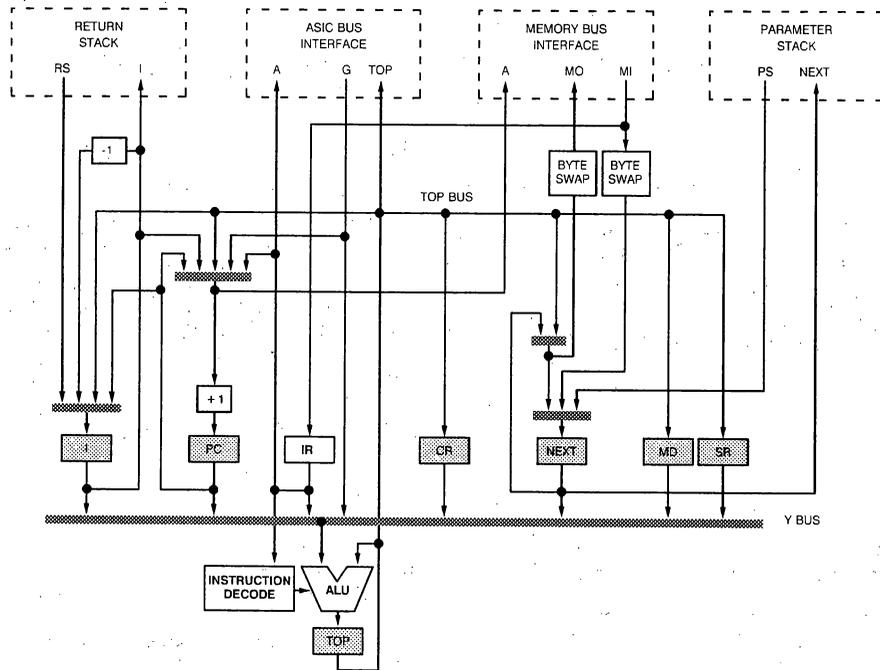
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# RTX SEMINAR



## RTX CORE PROCESSOR



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# RTX SEMINAR



## RTX 2000 - ON-CHIP STACKS

- Parameter Stack: 256 x 16 Bits
  - Top Register, Next Register, Parameter Stack Memory
- Return Stack: 256 x 21 Bits
  - Index Register, Return Stack Memory
- Stack Controllers (2)
  - Generate Stack Memory Addresses, Stack Error Interrupts

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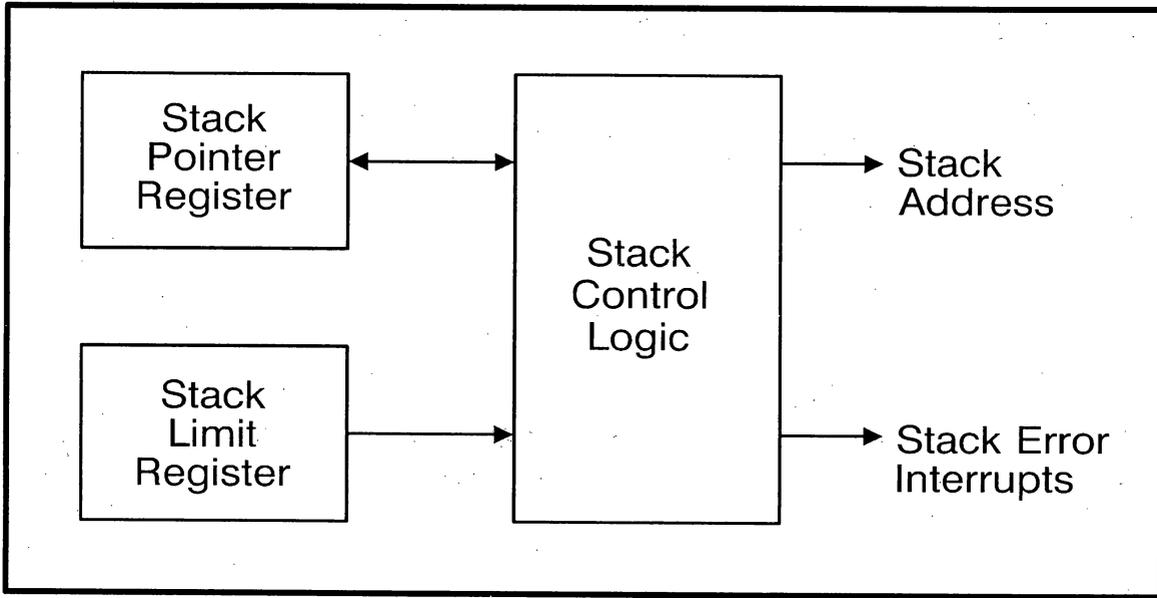
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# RTX SEMINAR



## RTX 2000 - ON-CHIP STACK CONTROLLERS



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# RTX SEMINAR



## RTX 2000 - ASIC BUS INTERFACE

- Extension of Internal Bus
- High Speed Peripheral Bus
- Communication Path to Other Processors

0189-029



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## RTX 2000 - HIGH SPEED I/O

- ASIC Bus
  - Operates Concurrently with the Main Memory Bus
  - 160 Mbit/Sec Transfer Rate
  - Concurrent ALU Operations Possible

0189-030

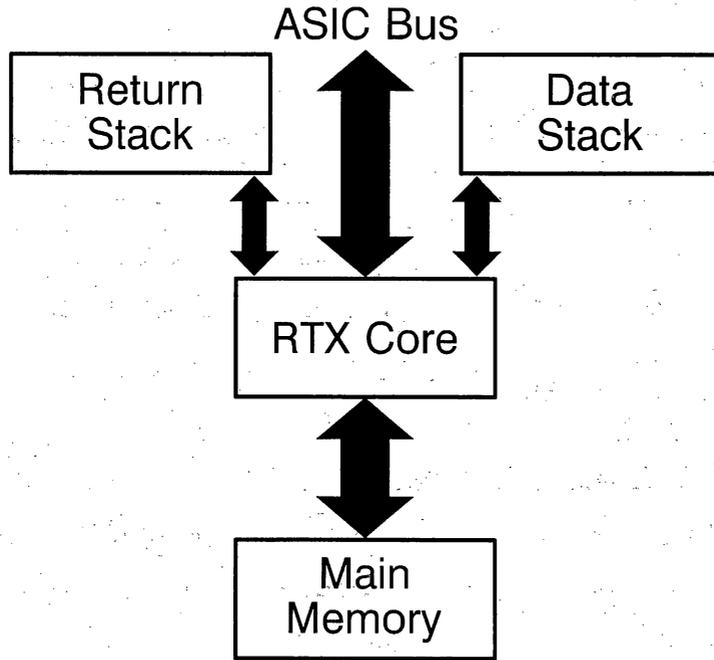


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# RTX SEMINAR



## RTX DUAL STACK, QUAD BUS™ ARCHITECTURE



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# RTX SEMINAR



## RTX 2000 - ON-CHIP INTERRUPT CONTROLLER

### INTERRUPT CONTROLLER

- Prioritizes Interrupt Requests
- Forwards Highest Priority Interrupt Request to Core
- Generates Interrupt Vectors

### INTERRUPTS

- Can Be Disabled by Core
- Can Be Individually Masked by Interrupt Controller
- Can Be Suppressed by Internal or External Hardware

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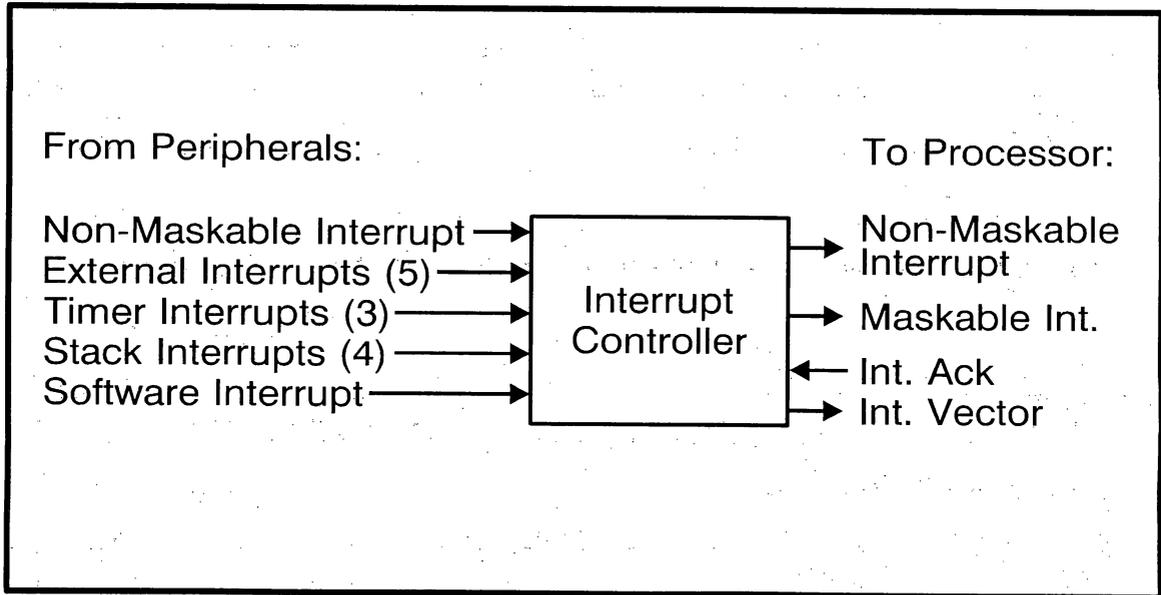


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# RTX SEMINAR



## RTX 2000 - ON-CHIP INTERRUPT CONTROLLER



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# RTX SEMINAR



## RTX 2000 - ON-CHIP TIMER/COUNTERS

- 3 Identical 16-Bit Count Down Counters
- Clocked with Internal Clock or External Inputs
- Reload and Generate Interrupt on Time Out

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# RTX SEMINAR



## RTX 2000 - LOW POWER

- Fully Static CMOS Design
  - 7 mA/Mhz Operation
  - 500  $\mu$ A Standby
- 6 Times Less Power Consumption Than RISC Processors at Full Speed
- 1000 Times Less Power Consumption Than RISC Processors When Idle

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# RTX SEMINAR



## WHAT THE RTX 2000 CAN DO FOR YOU

- Simplify Design
  - Reduce Parts Count
  - Simple Connections to Memory and Peripherals
- Increase Reliability
  - Fewer Parts
  - Less Heat

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# RTX SEMINAR



## WHAT THE RTX 2000 CAN DO FOR YOU

- Decrease Power Requirements
  - Low Power CMOS
  - Fully Static Operation
  - System Clock Can Be Slowed or Stopped
  
- ASIC Designability
  - On-Chip Custom Circuits
  - On-Chip Program ROM/RAM
  - Algorithms in Silicon

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# RTX SEMINAR



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## APPLICATION EXAMPLES

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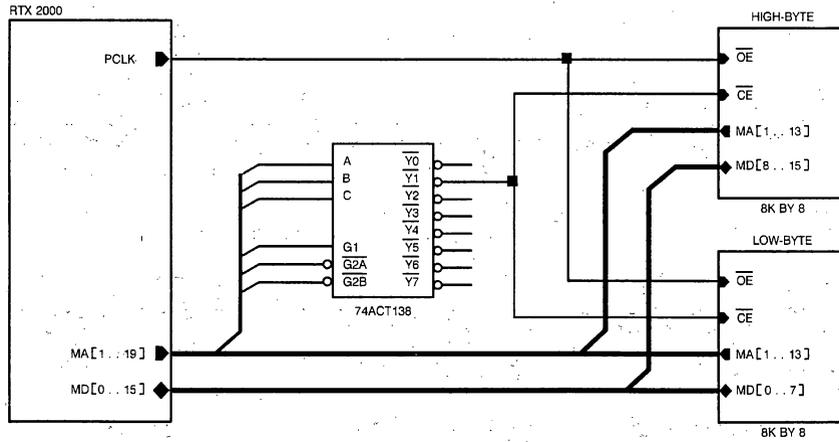


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# RTX SEMINAR



## RTX 2000 - EPROM INTERFACE



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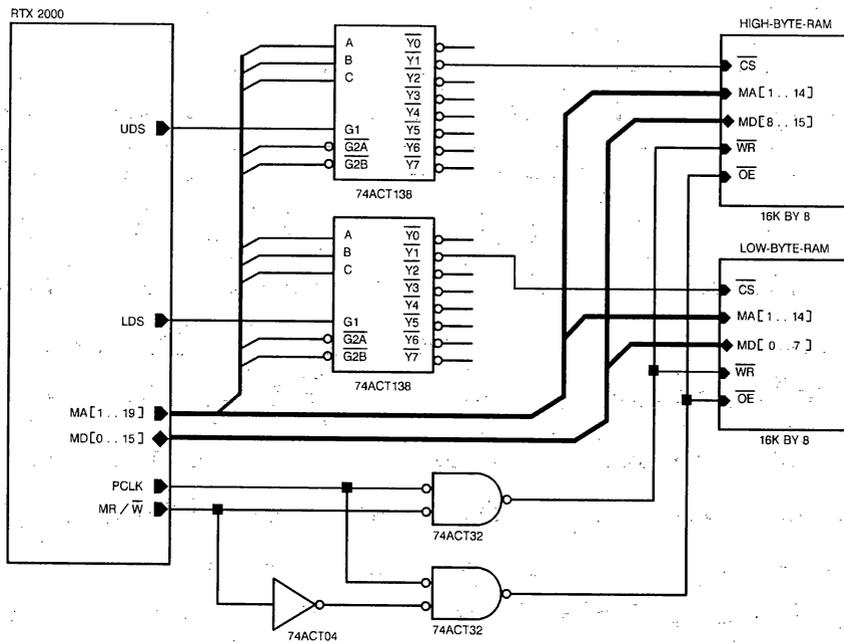


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## RTX 2000 - STATIC RAM INTERFACE



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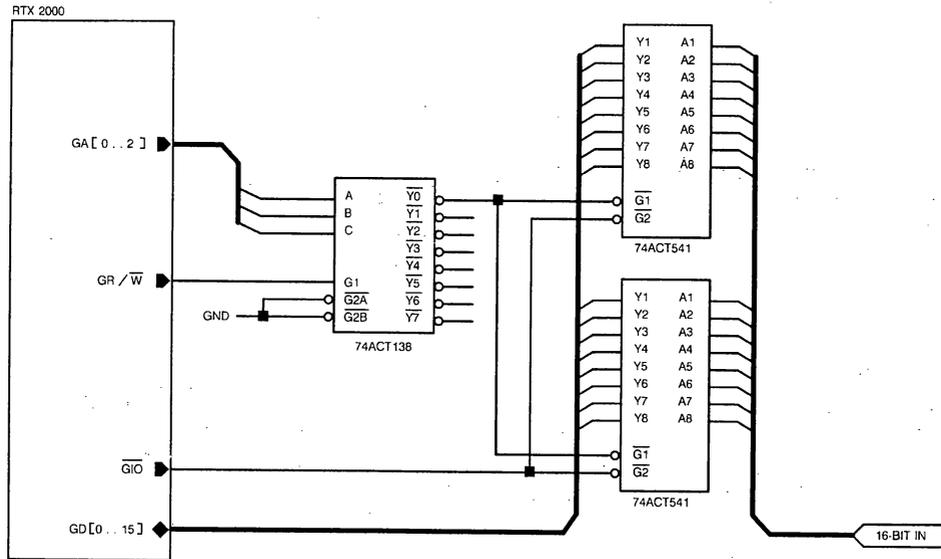
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# RTX SEMINAR



## RTX 2000 - 16-BIT PARALLEL INPUT PORT



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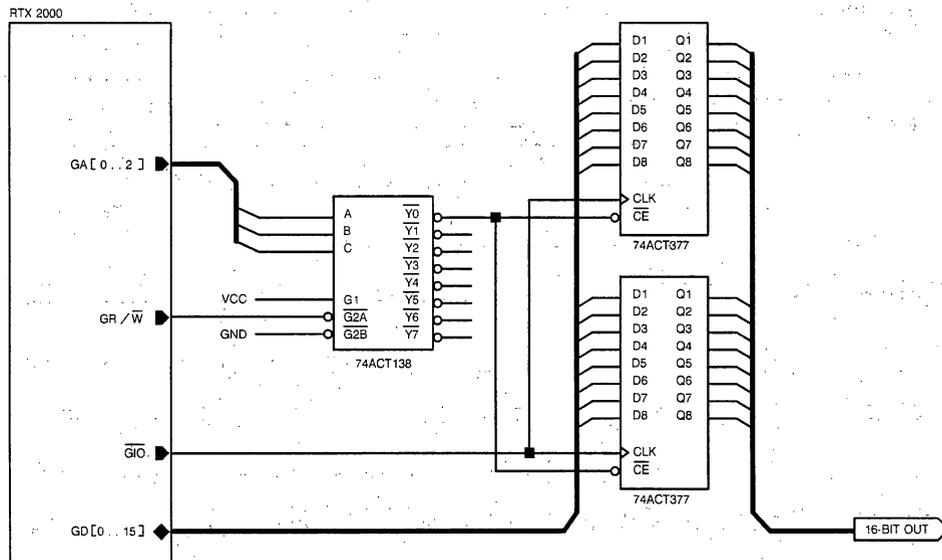


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# RTX SEMINAR



## RTX 2000 - 16-BIT PARALLEL OUTPUT PORT



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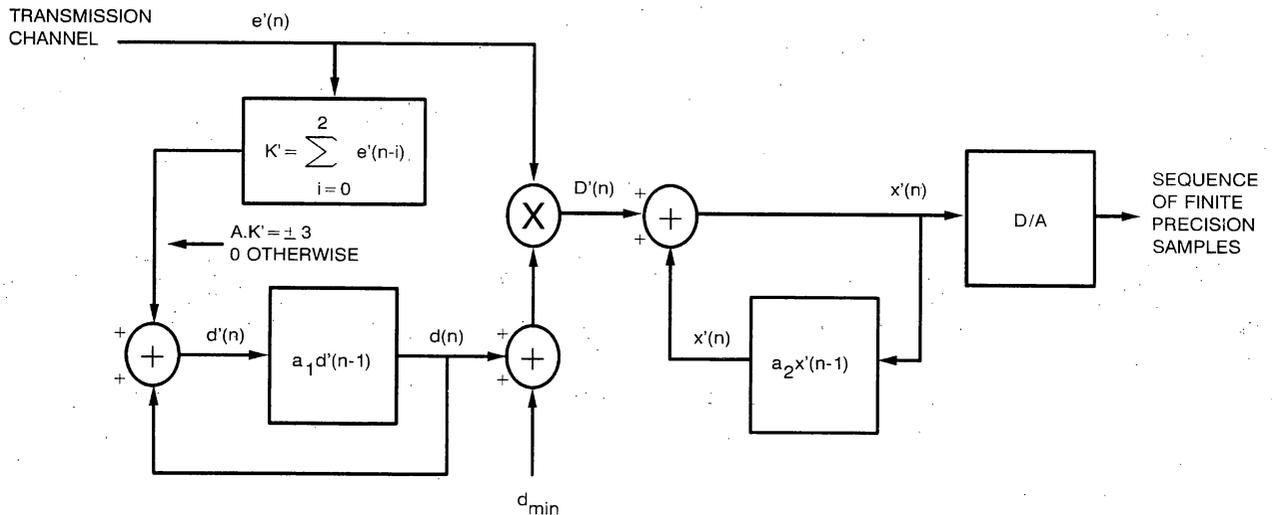


# RTX SEMINAR



## RTX 2000™ - VOICE/SPEECH COMPRESSION APPLICATIONS

### CVSD DECODER



0189-050

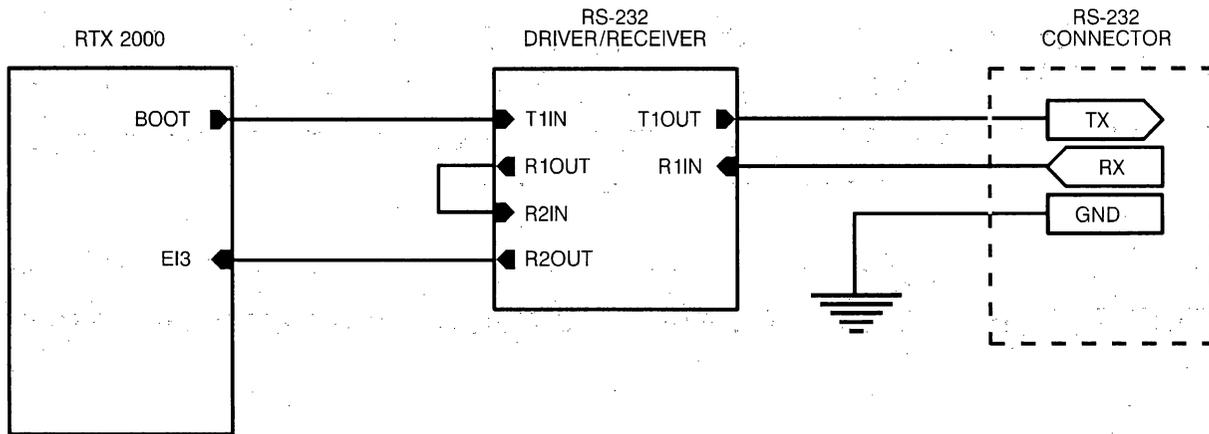


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# RTX SEMINAR



## RTX 2000 - SOFTWARE UART



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# RTX SEMINAR



REAL TIME EXPRESS

## HARRIS RTX VS ALTERNATE SOLUTIONS

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# RTX SEMINAR



## COMPETITIVE COMPARISON

Competitive Product Selection Based On

- Industrial Use in Real Time Control
- Manufacturers' Claims
- High Performance Processing Ability
- General Purpose Processors

0189-054



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# RTX SEMINAR



## COMPETITIVE COMPARISON

### Performance Data Presented in Cycles

- Permits "Apples-to-Apples" Comparison
- User Can Do Comparison Based on His Cycle Time
- Eliminates Benchmark Subjectivity

0189-055



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# RTX SEMINAR



## INTEGER MULTIPLY

	<u>Clock Cycles</u>
RTX 2000	1
Intel 80960	9 - 21
Intel 80286	13 - 24
Intel 80196	14 - 23
Am 29000	18 - 34
Motorola 68020	25 - 28
NEC V25	39 - 48
National HPC	58 - 76

0189-057



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# RTX SEMINAR



## PIN COUNT

	<u>Pin Count</u>
RTX 2000	84
Intel 80960	132
Intel 80286	68
Intel 80196	68
Am 29000	169
Motorola 68020	114
NEC V25	84
National HPC	68

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# RTX SEMINAR



## ASIC CAPABILITY

RTX 2000	Yes
Intel 80960	No
Intel 80286	No
Intel 80196	No
Am 29000	No
Motorola 68020	No
NEC V25	No
National HPC	Yes

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# RTX SEMINAR



## RTX 2000 VERSUS INTEL 80960

	<u>RTX 2000</u>	<u>Intel 80960</u>
Integer Mult.	1 Clock	9-21 Clocks
Move Block	2 Clocks/Word	6 Clocks/Word
Call/Return	1-2 Clocks	16-64 Clocks
Interrupt Latency	4 Clocks	100 Clocks
Pin Count	84	132

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# RTX SEMINAR



## RTX 2000 VERSUS 68020

	<u>RTX 2000</u>	<u>68020</u>
Instruction Set	RISC	CISC
Pipelined	No	3-Stage
Integer Mult.	1 Clock	25-28 Clocks
Move Block	2 Clocks/Word	6-9 Clocks/Word
Call/Return	1-2 Clocks	34 Clocks

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# RTX SEMINAR



## RTX 2000 VERSUS INTEL 80196

	<u>RTX 2000</u>	<u>Intel 80196</u>
Clock Rate	10 MHz	12 MHz
Integer Add	1 Clock	4-10 Clocks
Integer Mult.	1 Clock	14-23 Clocks
Move Block	2 Clocks/Word	8 Clocks/Word
Call/Return	1-2 Clocks	22-27 Clocks
Interrupt Latency	4 Clocks	16-18 Clocks

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# RTX SEMINAR



## RTX 2000 VERSUS NATIONAL HPC

	<u>RTX 2000</u>	<u>National HPC</u>
Clock Rate	10 MHz	8.5 MHz
Integer Add	1 Clock	6-21 Clocks
Integer Mult.	1 Clock	58-76 Clocks
Move Block	2 Clocks/Word	11 Clocks/Word
Call/Return	1-2 Clocks	14-21 Clocks
Interrupt Latency	4 Clocks	11 Clocks
Registers	Invisible	Only 6

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# RTX SEMINAR



## WHO IS THE RTX 2000 FOR?

### CUSTOMERS WHO REQUIRE

- Outstanding Performance
- Reduced Cost
- Predictable Execution
- Low Power Requirements
- Compact Code
- A Family of Possible Solutions
- A Semicustom Migration Path

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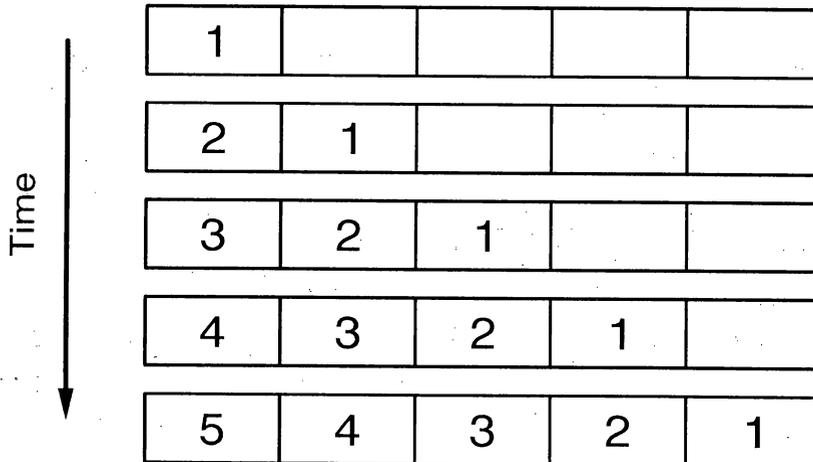
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# RTX SEMINAR



## PIPELINE OVERHEAD

### 5 STAGE PIPELINE



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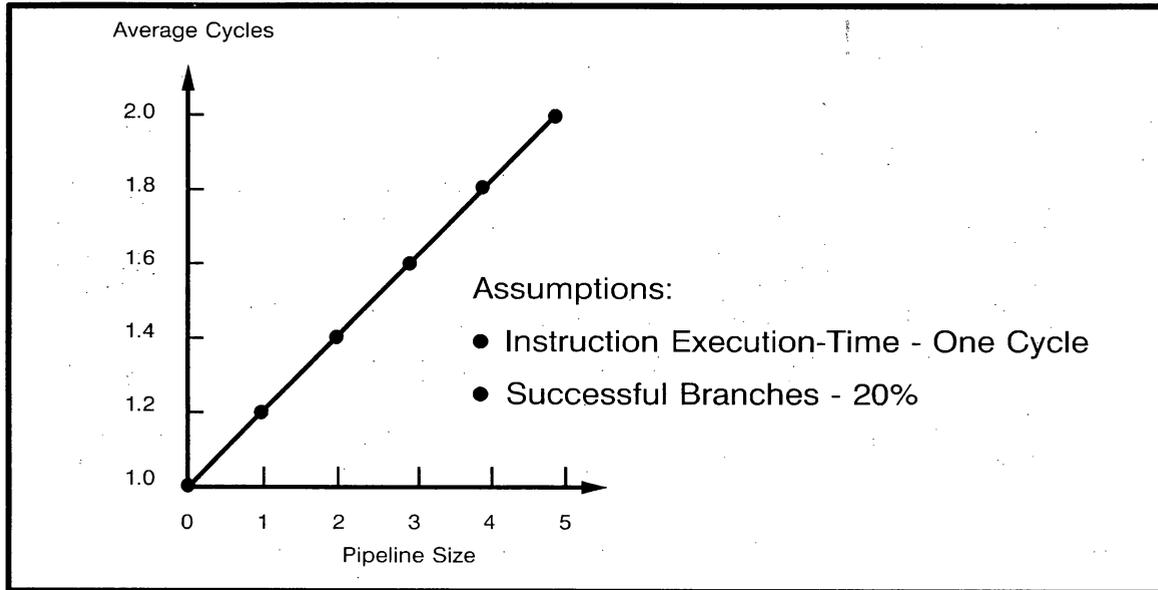


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## PIPELINE OVERHEAD



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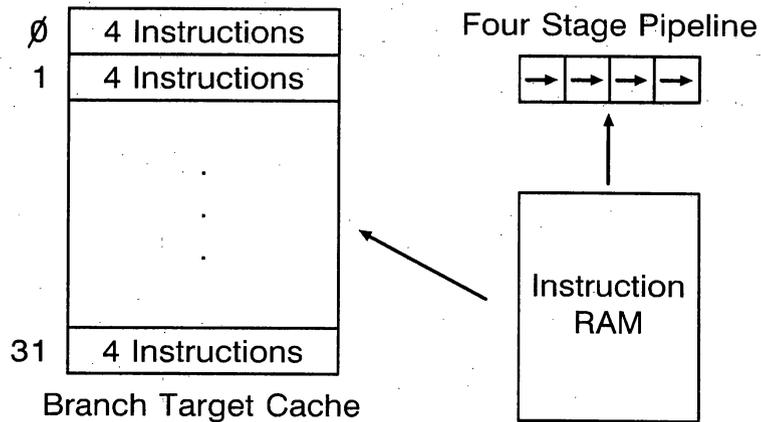


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# RTX SEMINAR



## BRANCH TARGET CACHE



### DRAWBACKS:

- Cache Miss on Initial Branches
- Not Predictable
- Must Design for Worst Case

0189-072



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## THE ALTERNATIVES

Cost	Much More
Integer Add	1-6 Times Slower
Integer Mult.	10-75 Times Slower
Move Block	3-8 Times Slower
Call/Return	10-50 Times Slower

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# RTX SEMINAR



REAL TIME EXPRESS

## DESIRABLE FEATURES OF DEVELOPMENT ENVIRONMENTS

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# RTX SEMINAR



## INTERACTIVITY

- Allows Programmer to Interact Directly with the Execution of the Software Application
- Benefits of Interactivity
  - Ability to Test Each Subroutine as Created
  - Fast Prototyping
  - Changes to Software Available Immediately
  - Promotes Bottom Up Implementation and Test

0189-078



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# RTX SEMINAR



## OTHER FEATURES

- Inexpensive, Easily Obtainable Host Computer
- Ability to Test Code Without Target Hardware
- Debugging Support
  - Full Speed
  - Symbolic
  - On-Line Source Code
  - Interactive

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REAL TIME EXPRESS

## PROGRAMMING LANGUAGES FOR REAL-TIME SYSTEMS FORTH AND "C"

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## WHAT IS FORTH

- FORTH Is a High Level, Interactive, Extensible Programming Language
- The Programmer Creates New Subroutines, or "Words" Which Become Part of the Language
- New Words Can Be Used Interactively or To Build Higher Level Words
- The End Product Is a Language Describing the Problem Being Solved

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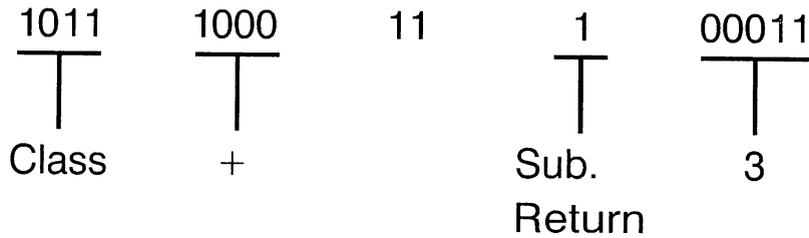


# RTX SEMINAR



FORTH ON THE RTX 2000™

: ADD\_3 3 + ; = 3 FORTH Instructions  
= 1 RTX Instruction



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## DEVELOPMENT ENVIRONMENTS

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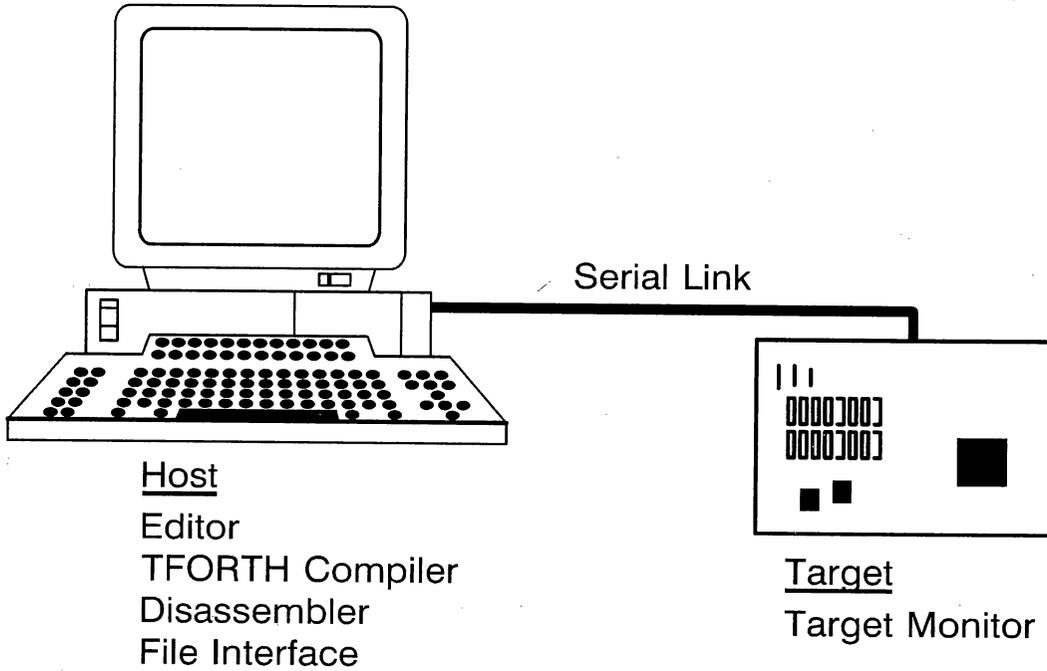
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## RTXDS CONFIGURATION

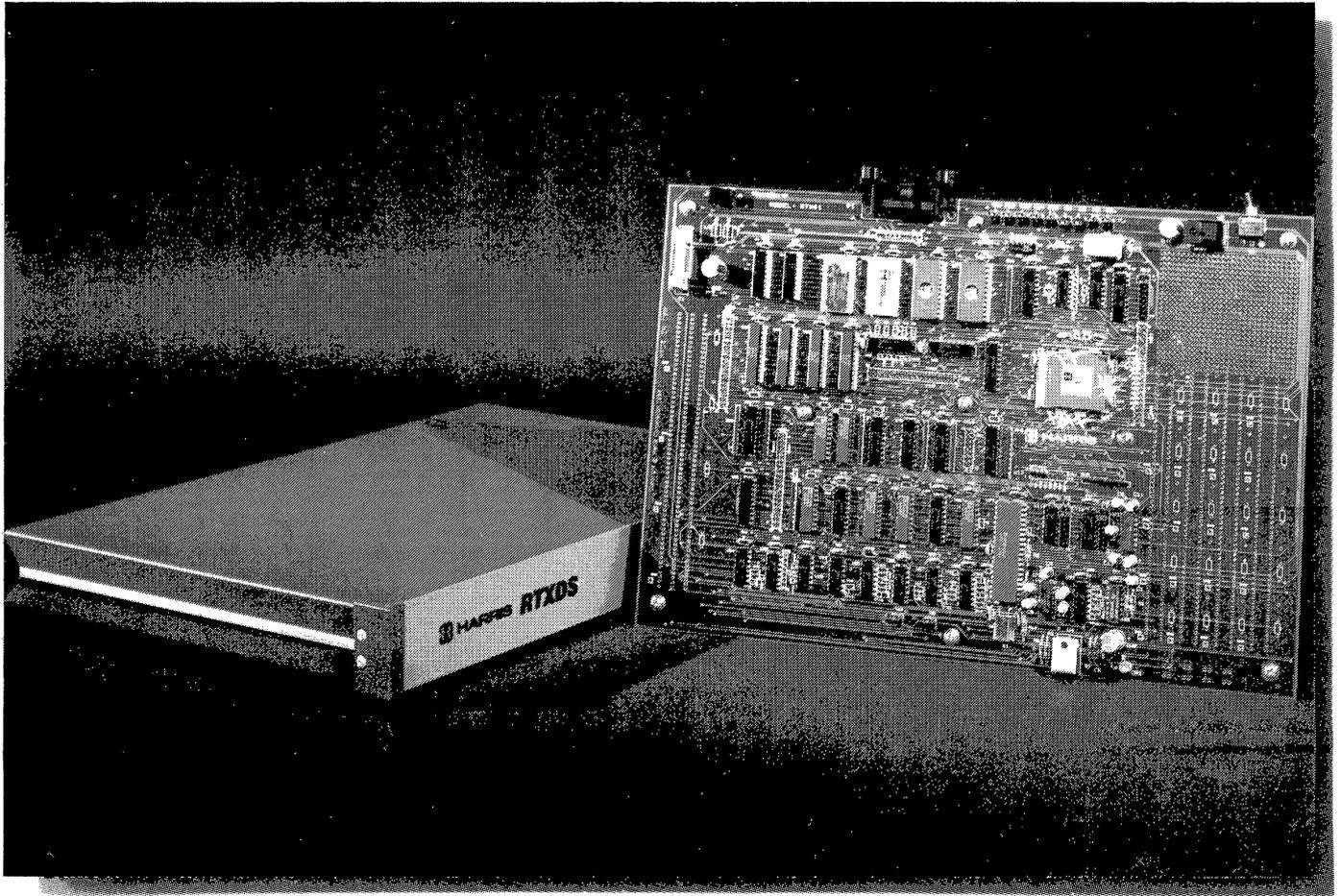


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## RTXDS CROSS COMPILER - TFORTH

- Cross Compiles FORTH-83 Compatible Source Code to RTX ROMable Machine Code
- Optimizes for RTX Architecture
- Designed to Support Embedded Control Systems
- Provides Support for RTX Features

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## RTXDS DEBUG MONITOR

- Debugging Features
  - Download Program Code
  - Examine/Change Memory, Registers, I/O Ports
  - Set Breakpoints
  - Monitor Memory Addresses
- Real-Time Debugging at Full Speed
- Symbolic Debugging
- Source Code and Compiled Code Available On-Line

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## MULTI-TASKING KERNEL

- Real-Time Operating System Kernel
  - Features
    - Pre-Emptive Multi-Tasker
    - Prioritized Task Scheduling
    - Inter-Task Communication
    - Memory Management
    - Resource Management
    - Interrupt Handling
  - Real-Time Debugging Tools Will Be Included

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## RTX 1553 - 1553 INTERFACE/CONTROLLER

- Operates on RTX Memory or ASIC Bus Without Wait States
- Dual Redundant 1553 Buses

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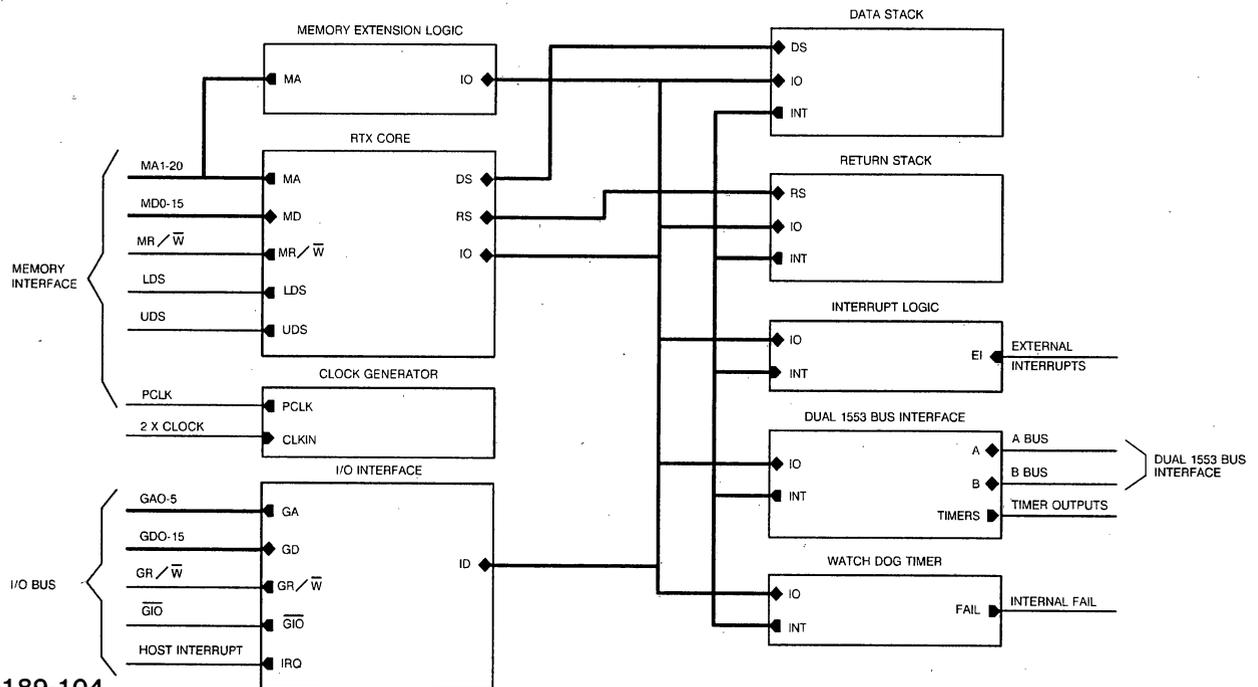


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## RTX 1553 FUNCTIONAL BLOCK DIAGRAM



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## RTX 2152 HIGH SPEED BUS UART

- Operates on RTX Memory or ASIC Bus Without Wait States
- Software Compatible with 82C52

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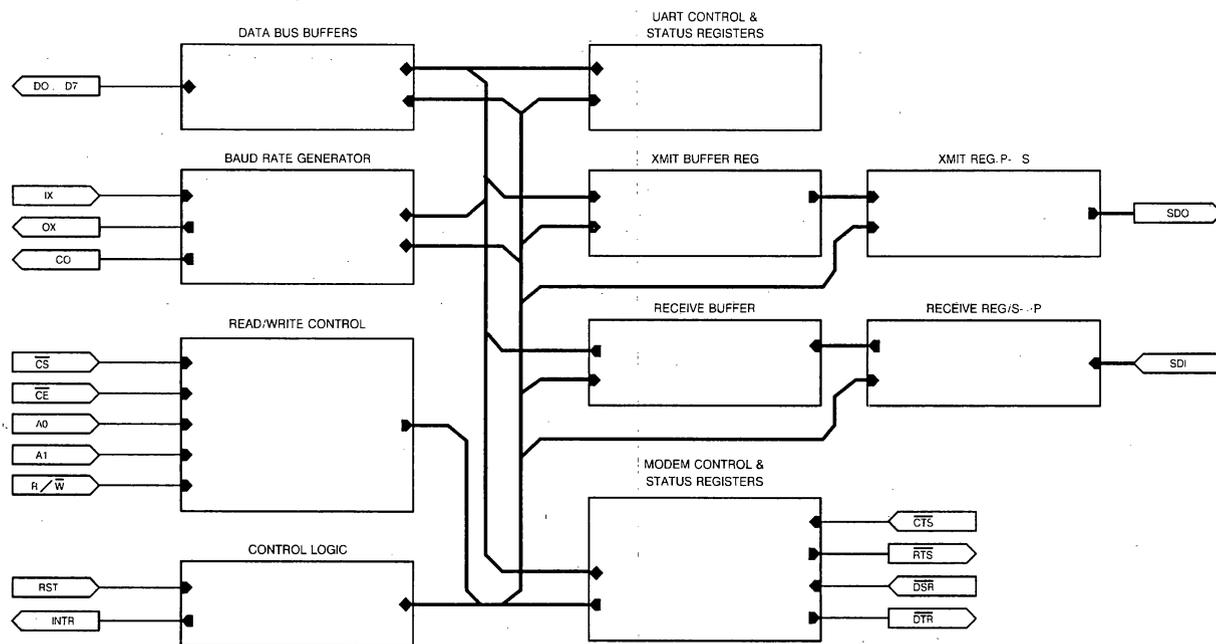


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## RTX 2152 FUNCTIONAL BLOCK DIAGRAM



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## RTX DEVELOPMENT SYSTEM

- RTXDS-10: 10MHz

## RTX DEVELOPMENT BOARD

- RTXDB-10: 10MHz
- RTXDB-8: 8MHz

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## OPTIMIZED COMPILERS

- FORTH - Now
- C - 1st Quarter, 1989
- Prolog - 2nd Quarter, 1989

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SILICON COMPOSERS

- SC/FOX™ System
- SC/FORTH™ Language
- Development Services

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## ADDITIONAL THIRD PARTY SUPPORT

- Surrey Medical Imaging Systems
  - RTX2000 Pulse Processor
  - Software Support
- Others

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