Threshold Voltage Assignment to Supply Voltage Islands in Core-based System-on-a-Chip Designs

Steven Beigelmacher  
steven7@ece.cmu.edu

Gall Gotfried  
 ggall@andrew.cmu.edu

ABSTRACT
Circuit-level techniques, particularly supply and threshold voltage assignments, are among the most effective in designing for low power. However, the conflicting effects of supply and threshold voltage assignments require an integrated approach in determining these values. Furthermore, the realities of increasingly large and complex designs means we may no longer have the freedom to tweak process parameters at the level of individual gates. The use of voltage islands in a core-based SoC design seems like a natural extension to the circuit-level techniques we are already familiar with. Here we propose to take the description of an existing supply voltage island partitioner/placer and enhance it to take threshold voltages into account. We would also like to add to the tool a notion of required performance characteristics for different cores that make up an SoC.

1. INTRODUCTION
Advances in process technology and decreasing feature size have been the bread and butter of the semiconductor industry, permitting a steadily increasing number of integrated devices on a chip. As devices grow smaller and designs become more complex, component integration has moved from beyond standard cells and memory macro blocks to entire cores. This type of design, known as System-on-a-Chip (SoC) design, revolves around the idea of using existing processing elements (PEs) and memories, and connecting them in some bus-based topology. PEs come in several flavors, such as simple processors, DSP functions, or even application-specific hardware. The application of the SoC design is realized by the selection of different PEs and memories, the communication that exists between them, and the programming of the PEs. We believe that with IP offerings growing more robust and greater consumer expectations requiring more complex design, we will continue to see SoC designs play a prominent role in the design space.

While performance has dominated the design focus for so long, minimizing power consumption is playing an increased role in the design space. This is just as true in the enterprise server space as it is in the mobile electronics space. The same trends that have enabled unheralded levels of device integration have also served to make the power problem more severe. Decreasing feature size comes with a decrease in the baseline supply voltage, placing a limit on the usefulness of future supply voltage assignment techniques. Furthermore, the increasing number of devices on a chip has made the problem of static power consumption even more immediate. As a result we need to be mindful of both voltages. We wish then to find a solution to the power problem that takes both supply and threshold voltage into account, in the context of a core-based SoC design.

2. RELATED WORK
Previous works attempted to reduce power consumption in a physically-constrained core-based SoC design [1]. In this study, the authors considered an SoC design with a set number of cores inside of a given die size. Each core either had required dimensions or required area with a minimum aspect ratio. Each core also had a set of acceptable supply voltages that might be used for that core. The authors proposed a tool that begins working after an initial placement of these cores had been completed. Some of the cores are designated as fixed, other cores may be moved around the die.

The tool developed by the authors sought to create voltage islands, regions where cores using the same supply voltage were placed in close proximity to one another. Cores are re-placed if a new placement will create larger voltage islands. In some cases a core will operate at a supply voltage other than its minimum in order to fit into a voltage island. The problem is solved using simulated annealing, with a cost function that emphasizes moving cores operating at the same supply voltage closer to one another. Perturbations include splitting a voltage island into two smaller islands and setting all cores that may operate at a random supply voltage to that level. Within islands, local placement is done to reduce the amount of dead space. PEs come in several flavors, such as simple processors, DSP functions, or even application-specific hardware. The application of the SoC design is realized by the selection of different PEs and memories, the communication that exists between them, and the programming of the PEs. We believe that with IP offerings growing more robust and greater consumer expectations requiring more complex design, we will continue to see SoC designs play a prominent role in the design space.

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Other related work deals with supply voltage selection on a more fine-grained scale [2]. Instead of partitioning the cores based on supply voltage the authors look at the gate...
level implementation to cluster regions of the chip. Here the number of voltage converters is also minimized but the balance of Vth and Vdd is always kept to have performance at a maximum.

The performance requirements of a system are also enforced by taking the approach of frequency islands [3]. The cores are partitioned according to the minimum frequency at which they can operate but the inter-core communication becomes a significant factor. By analyzing the size of the communication queues and relating them to the amount of work transferred between cores the authors came up with a converging algorithm to reduce power by running cores at the lowest frequencies.

3. DESIGN SPACE
We propose to take previous works in supply voltage assignment to core-based SoC designs and extend those solutions to take threshold voltage assignment into account. Due to the increasing percentage of power consumption that is made up of static power dissipation, we feel that this is a worthwhile endeavor. Because previous solutions [1] remain closed, our first step will be to implement the algorithm that only works with supply voltage assignment so that we may have some basis for comparison.

Additional considerations in our algorithm will have to account for the varying latencies. As changing the threshold voltage and supply voltage different islands may be forced to run at different frequencies. We will attempt to balance the two voltages as in [2] to keep the entire system running at the minimum frequency to reduce power.

We are considering several approaches in the combination of Vdd and Vth assignment. One such approach is to run our algorithm to repartition the already partitioned Vdd islands to optimize for Vth. This will in turn run our algorithm after the supply voltage assignment. Another such approach is to run the two phases simultaneously. Here we can partition partly with respect to Vdd assignments and then partly with Vth assignments. Finally, the last consideration is partitioning initially with respect to Vth and then considering supply voltage. Our experiments will evaluate which approach will achieve minimum islands with least power consumption.

4. MILESTONES
4.1 Explore Previous Work -- 02/23/2005
For this milestone we will attempt to better understand the workings of the baseline algorithm presented in [1] and begin a new implementation. This is necessary so that we may perform comparisons to evaluate our changes.

4.2 Extend Algorithm -- 03/21/2005
Complete previous algorithm implementation and gather results based on benchmarks, which we will also need to create. Begin its extension to include threshold voltage assignment.

4.3 Complete Algorithm and Achieve Results -- 04/11/2005
Complete algorithm with threshold voltage assignment and evaluate the optimal approach, as discussed in section 3. Use this approach to gather data and results for the given benchmarks.

5. REFERENCES