PageRank Acceleration for Large Graphs with Scalable Hardware and Two-Step SpMV

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Research Problem
PageRank is a widely used iterative algorithm that ranks the vertices of a graph according to their relative importance. However, it suffers from poor performance and efficiency due to notorious memory access behavior. More importantly, when graphs become bigger and sparser, PageRank applications are inhibited as most solutions profoundly rely on large random access fast memory, which is not easily scalable.

Solution
We designed a 16nm ASIC (currently under fabrication) based shared memory platform for PageRank that fundamentally accelerates Sparse Matrix dense Vector multiplication (SpMV), the core kernel of PageRank.

ASIC for PageRank
16nm FinFET
ASIC for
PageRank

PageRank Acceleration (currently being fabricated)

Key Goals
- Streaming DRAM access
- Full utilization of streaming bandwidth
- Off-chip DRAM traffic reduction
- Low requirement of fast on-chip memory (scalability)

Two-Step SpMV

This algorithm conducts SpMV in two separate steps. It requires column blocking of the matrix and segmentation of the source vector.

Two-Step SpMV Algorithm

Segment width depends on fast memory

Less Dependence on SRAM - More Scalable

Solution

Fast memory (MB)  Max. nodes reported

FPGA [3]  8.4  2.3M
ASIC [4]  32  8M
CPU (single socket) [5]  20  95M
CPU (single socket) [6]  50  118M
PR_TS_Opt (proposed)  11  28
PR_TS (proposed)  11  48

Background on SpMV
SpMV, the core operation of PageRank, requires random access to dense vector which is too large for the last level cache. This results in random access to DRAM, affecting performance and efficiency in many ways. Below is a comparison of required vs redundant data transfer and dram page openings of baseline SpMV on a example problem. Example: 80M x 80M matrix, 3 NNZ per row, 1GB DRAM page, 64B cache block, double precision data

Data Volume - 15GB
Required 37%
Redundant 43%

Performance & Efficiency

- PageRank Performance & Efficiency

PageRank vector: \( \mathbf{x} = \mathbf{A} \mathbf{x} + (1 - \alpha) \mathbf{v} \)

Two-Step SpMV

The two-step SpMV algorithm is conducted independently in each iteration of PageRank. The resultant vector of one iteration is the source vector of the next, communicated via DRAM. The Step 2 is conducted at any given time, keeping other part of the circuit inactive.

Optimized PageRank by Iteration Overlap (PR_TS_Opt)

Two source vector segment storages in fast memory are required: (1) for computation of Step1 in iteration i and (2) for storing output of Step 2 in iteration i.

Optimized Two-Step driven PageRank (PR_TS_Opt) attains much higher throughput with the same silicon area and saturates HBM's extreme off-chip bandwidth.

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Experimental Results

- Streaming speed PR_TS
  - Src. vec. load (step 1): 346 GB/s
  - Partial SpMV (step 1): 297 GB/s
  - Merge (step 2): 432 GB/s
  - Final speed PR_TS_Opt: 729 GB/s

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