Si-Ge-C Growth and Devices

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ABSTRACT

Silicon-germanium can now be regarded as a relatively well-established technology, and consequently much recent work has addressed the additional possibilities opened up by adding carbon to form the ternary alloy SiGeC. Carbon in principle provides additional bandgap engineering possibilities and also has an important impact on the stability of strained epitaxial layers. This paper surveys recent work on the growth of Si-Ge-C epitaxial layers, with particular emphasis on the advantages and limitations of carbon incorporation. Examples of applications in which carbon leads to improved device performance are discussed.

1. Introduction

The heterojunction bipolar transistor was described in Shockley's patent of 1951[1], and semiconductor heterojunctions have been very important in III-V devices. But despite the importance of the heterojunction concept, its successful application to silicon-based devices is rather recent. The silicon-germanium base heterojunction bipolar transistor was first demonstrated in 1987 [2] and it is only now becoming a well-established device technology.

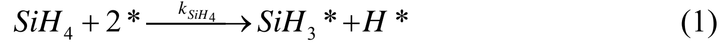
It is natural, then, to explore other column-IV heterostructures. One area of recent investigation has been the ternary Si-C-Ge system. The materials problems here are very challenging; however, there appear also to be new device applications for which the binary Si-Ge alloy is not completely satisfactory. This paper reviews some of the obstacles to the growth of carbon-containing materials and, in particular, the practical limits of carbon incorporation. Recent work on novel devices in this material system is then reported, emphasizing field effect devices.

2. Growth of Ternary Si-Ge-C Alloys

The lattice constant of germanium differs from that of silicon by only about 4%, and the germanium-silicon phase diagram is an ideal isomorphous phase diagram. Consequently growth of strained layers of $Si_{1-x}Ge_x$ on silicon is practical over a wide compositional range. For low germanium content the thickness of epitaxial layers is limited by the formation of misfit dislocations, which can form either during growth or during subsequent high-temperature annealing. For higher germanium content the onset of undulated growth is more likely to limit the practical range of epitaxial layer thicknesses. In both cases, low temperature growth is highly desirable; and as a result, there has been considerable research into growth by molecular beam epitaxy (MBE) and low-temperature chemical vapor deposition (CVD). Under appropriate growth conditions, both MBE and CVD techniques are capable of growing device-grade layers. However, CVD techniques are much more acceptable in production and in addition have the advantage of a significant hydrogen coverage of the surface during growth.

A brief summary of the surface reactions during growth by CVD is necessary to understand the growth of carbon-containing layers. Figure 1a,b summarizes reactions of

SiH_4, GeH_4, and H_2 on a silicon (100) surface[3]. Chemisorption requires two vacant sites, with the initial surface reactions given by



$$SiH_4 + 2* \xrightarrow{k_{SiH_4}} SiH_3* + H* \quad (1)$$

$$H_2 + 2* \xrightarrow{k_{H_2}} 2H* \quad (2)$$

where * indicates a vacant site and X* the species X on a vacant site. The SiH_3* species rapidly decomposes yielding additional SiH* on the surface or hydrogen molecules. The SiH* species are more stable, and hydrogen is liberated from the surface by the reaction

$$H* \xrightarrow{k_d} \tfrac{1}{2} H_2 + * \quad (3)$$

Consequently epitaxial layer growth is limited at low temperatures by hydrogen desorption (which is thermally activated) and at high temperatures by the supply of reactant. The rate at which reactant molecules are decomposed is given by

$$R = Z_{SiH_4} s_{SiH_4} \Theta^2 \quad (4)$$

where Z_{SiH_4} is the silane flux, Θ is the fraction of surface sites not occupied by hydrogen, and s_{SiH_4} is known as the reactive sticking coefficient, and is approximately 4×10^{-3} for silane. Hydrogen can also decompose on the surface and consequently has the effect of reducing the number of active sites. As its sticking coefficient is substantially smaller than most commonly used reactants ($s_{H_2} = 2 \times 10^{-5}$) its effect is significant only at relatively high partial pressures.

This discussion provides a framework for understanding the growth of both $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$. Germane (GeH_4) behaves similarly to silane except that its sticking coefficient is somewhat higher and the presence of germanium on the surface increases the hydrogen desorption rate. Consequently growth rates are increased by the addition of germane. Germane competes with silane for the same active sites; the germanium fraction is given by

$$x = \left(1 + \frac{M_{GeH_4}}{M_{SiH_4}} \frac{s_{SiH_4}}{s_{GeH_4}} \frac{p_{SiH_4}}{p_{GeH_4}} \right)^{-1} \quad (5)$$

In some cases, other silicon reactants are used. Disilane (Si_2H_6) is similar to silane in that it requires two active sites for the initial surface reaction. Dichlorosilane (SiH_2Cl_2) is somewhat more complex (Fig. 1c) since its decomposition results in surface chlorine. This chlorine can be removed from the surface as HCl or alternatively as $SiCl_2$, which results in no net deposition. Consequently growth from dichlorosilane requires a hydrogen ambient and growth rates are generally lower in the low-temperature regime. As will be discussed later, carbon reactants cause a decrease in growth rate, and consequently dichlorosilane is not an attractive reactant for growth of carbon-containing layers.

$Si_{1-x-y}Ge_xC_y$ is of interest only because carbon can be incorporated substitutionally in concentrations far greater than its equilibrium solubility. This can was observed in early work by MBE [4] and has been attributed to the enhanced solubility of carbon in particular subsurface sites[5]. In the case of growth by MBE, Osten and coworkers [6] have proposed a model in which carbon is first incorporated substitutionally in subsurface sites and subsequently can form interstitial defect complexes by a thermally activated process. This model explains the reported decrease in substitutional carbon concentration with increasing growth temperature (with constant germanium and carbon flux) and also the decrease in substitutional carbon concentration with increasing germanium fraction (with constant carbon flux and temperature).

It is now well known that the hydrogen present on the surface during CVD growth has beneficial effects, and this is also true for carbon incorporation. When comparing CVD and MBE growth of SiC at the same growth rate and temperature, higher substitutional carbon concentrations are obtained with CVD growth [7], and MBE growth in a hydrogen plasma also increases the substitutional carbon concentration [8]. These observations can be qualitatively attributed to the reduction of surface diffusion rate by surface hydrogen. Additionally, it is known that hydrogen termination causes an increase of 0.1 Å in the dimer bond length [9]. Possibly this favorably impacts the subsurface solubility of hydrogen. Antimony also acts as a surfactant and has a similar effect on the substitutional carbon concentration [10]. Fully substitutional carbon concentrations as high as 1.8% can be obtained at 550 C by CVD [11]. Figure 2 summarizes various reports of substitutional carbon concentration [7,11,12,13]. The highest fully substitutional carbon concentrations were obtained with high SiH_4 partial pressures [11]. Growth of $Si_{1-x-y}Ge_xC_y$ is generally similar in that there is a limited amount of carbon

which can be incorporated with full substitutionality. However, the maximum carbon concentration is somewhat less [14].

CVD growth also has some liabilities, however. The growth rate is strongly depressed by the addition of carbon-containing reactants (usually, but not invariably [15], methylsilane). Figure 3 shows the observed growth rate of $Si_{1-y}C_y$ in UHV/CVD as a function of total carbon mole fraction. The strong decrease in growth rate is consistent with other reports by RTCVD and LPCVD. The decrease is far stronger than one would expect based on the growth model discussed above. Just as germanium increases the hydrogen desorption rate, carbon in the epitaxial layer should decrease the hydrogen desorption rate due to the higher strength of the bond between hydrogen and carbon. However, a substantial decrease in growth rate is observed at bulk carbon concentrations which are still rather low-near 1% [7]. This suggests either higher concentrations at the surface than in the bulk (which is inconsistent with surface science studies [16] and with the picture of high solubility of carbon in subsurface layers) or that a single carbon atom can influence several surface sites. Alternatively, Ichikawa et al. [17] have suggested that reactants adsorb preferentially at Ge-Si pair sites, and thus a small carbon concentration might strongly alter the overall reaction rate. However, this picture cannot explain the fact that a strong decrease in growth rate also occurs during growth of $Si_{1-y}C_y$.

It is clear from the above discussion that there are severe limits on the amount of carbon that can be incorporated into $Si_{1-y}C_y$ or $Si_{1-x-y}Ge_xC_y$. In the case of MBE one must use very low growth temperatures (much less than 550 C) or very high growth rates in order to obtain substitutional carbon concentrations near 1%. In the case of CVD, growth temperatures near 550 C are required; however growth rates are already low at these temperatures and become even lower when carbon is incorporated. As a result, device design is very much constrained by the limitations of growth techniques-even more so than with $Si_{1-x}Ge_x$ devices. In following section, I will focus on the application of $Si_{1-x-y}Ge_xC_y$ to field effect devices.

3. $Si_{1-x-y}Ge_xC_y$ in MOSFET Devices

While much of the early work on $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ focused on HBT applications, recently the application of $Si_{1-x-y}Ge_xC_y$ to field effect devices has also been explored. In the following, I will summarize some recent work on both n-channel and p-

channel MOSFETs. This work is to a large degree motivated by the anticipated difficulties in meeting the objectives of the ITRI Roadmap, [18] specifically for drive currents for both n-channel and p-channel devices.

In n-channel devices, an improvement in performance can be obtained by using a compressively strained silicon channel. Here the effect of strain is to decrease the conduction band effective mass for in-plane transport and to decrease intervalley scattering. The consequence is an increase in both low-field mobility and the saturation velocity, as recently reported by Hoyt et al. for silicon-channel devices [19].

In order to create a strained silicon channel, it is necessary to grow a silicon epitaxial layer on a relaxed $Si_{1-x}Ge_x$ buffer layer (as was in fact done by Hoyt et al. [19]). The technology for growing relaxed $Si_{1-x}Ge_x$ buffers is well established; however, the buffer layer thicknesses required can be very large. A more attractive approach is to grow a compressively strained $Si_{1-y}C$ layer on a silicon substrate. In this case the band offset is almost entirely in the conduction band and is roughly given by [20]

$$\Delta E_C = 6.8y \quad [eV] \tag{6}$$

where ΔE_C is the conduction band offset and y is the carbon mole fraction. This device requires relatively high carbon concentrations in order to significantly alter the band structure of the $Si_{1-y}C$ layer. Unfortunately work to date has shown equal or reduced mobility compared to silicon channels [21].

We now consider p-MOSFET devices, where more encouraging results have been obtained. Figure 4 shows the device structure which has been explored by several groups. This is a heterostructure field effect device in which the holes are confined to a subsurface channel. Improved hole mobility is expected to result from (1) the decrease in effective mass due to the valence band and (2) decreased scattering from charges at the Si-SiO_2 interface. In some earlier work, the use of $Si_{1-x}Ge_x$ channels to fabricate improved p-channel transistors was explored by a number of researchers [22,23,24,25]. Improved channel mobilities were obtained and this was attributed to the altered effective mass in strained layers and also due to the greater distance between the channel and interface-related scattering centers. However, one limitation in this early work was the relaxation of the $Si_{1-x}Ge_x$ channel. When conventional thermal oxidation is used for the gate insulator, the channel must be less than the equilibrium critical thickness. This leads

to a severely constrained design space as high germanium fraction is desirable for carrier confinement and the channel needs to be thick enough to minimize the quantum confinement energy. Alternatively, channels greater than the equilibrium critical thickness can be used although a deposited gate insulator is then necessary.

Carbon-containing layers are beneficial in improving the process flexibility and in particular making it possible to use conventional thermal gate oxides and ion implant annealing. Strained carbon-containing alloys relax at higher temperatures than $Si_{1-x}Ge_x$ and by a different mechanism (SiC precipitate formation rather than dislocation generation) [26,27]. It was also found that carbon reduced the outdiffusion of boron [28], which limits spreading of the boron sheet doping. The first attempt to fabricate p-MOSFETs with carbon-containing channels was by John et al. [29], who used a 400 A $Si_{0.793}Ge_{0.2}C_{0.007}$ channel. They reported a maximum mobility for the $Si_{1-x-y}Ge_xC_y$ device of 160 cm^2/Vsec, which was only slightly higher than a surface-channel silicon device fabricated at the same time.

In subsequent work, Mocuta and Greve [30] studied $Si_{1-x-y}Ge_xC_y$ channels containing a smaller amount of carbon. Most previous work had focused on carbon concentrations of 0.5% or greater; however, beneficial effects are also observed at low carbon concentrations which are easier to achieve with UHV/CVD. Figure 5 illustrates the effect of thermal annealing on two UHV/CVD- grown strained layers, one containing 0.2 % carbon and the other an $Si_{0.91}Ge_{0.09}$ layer with comparable strain and thickness. The $Si_{0.888}Ge_{0.11}C_{0.002}$ layer begins to relax by formation of dislocations above about 650 C, while there is no change to the $Si_{1-x-y}Ge_xC_y$ layer up to about 900 C. Above this temperature, relaxation proceeds by formation of SiC precipitates, as evidenced by the shift of the layer peak away from the substrate peak. Reduced boron diffusion is also observed in such low-carbon materials.

Figure 6 presents results for a device with a channel 300 Å thick and containing 0.2% carbon. The germanium fraction was linearly ramped from 10% to 40%. In order to perform a reliable determination of the mobility, the source-drain capacitance technique [31] was used to measure the channel charge (open points) and the mobility (solid points) was then determined using the measured drain current in the linear regime. For comparison similar measurements on a silicon surface-channel device are also shown.

For low gate voltages (+0.1 > V_G > -0.5 V), holes are present only in the $Si_{1-x-y}Ge_xC_y$ channel and a mobility of about 200 cm^2/V·sec is measured. As the gate voltage is increased, the surface channel becomes occupied and the mobility drops to about 150 cm^2V·sec. Approximately the same mobility is observed in a silicon surface-channel device fabricated in the same process. This shows that $Si_{1-x-y}Ge_xC_y$ channels can provide an appreciable mobility enhancement. It should be emphasized that this device has a non-optimal vertical profile; in particular the silicon cap layer was quite thick in order to permit a very conservative process. In addition, the performance of short-channel devices is also influenced by the hole saturation velocity, which has not yet been measured. In recent work, Quinones et al. [32] reported improved drive current in $Si_{1-x-y}Ge_xC_y$ transistors with thinner silicon cap layers. The observed improvement in drive current was approximately 33%. Somewhat higher carbon concentrations were used (y = 0.005-0.007); however, they emphasize that best results were obtained for intermediate carbon concentrations.

4. Summary and Future Prospects

Recent work has shown two potential roles for $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ in MOS processes: as a relaxed buffer layer for n-MOSFETs and as a buried channel in p-MOSFETs. These devices can help to address the difficult on-current requirements for both transistor types in scaled CMOS processes. While formerly the thicknesses required for a relaxed buffer may have seemed an insurmountable obstacle, it is possible that SOI substrates will provide a practical solution. An intriguing example of how both types of devices can be fabricated is found in the paper by Mizuno et al.,[33] who use a relaxed $Si_{0.90}Ge_{0.10}$ SOI substrate to fabricate both n *and* p-channel devices using a single layer structure. It is therefore likely that scaled CMOS will incorporate $Si_{1-x}Ge_x$, $Si_{1-x-y}Ge_xC_y$ or both in future generations.

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Figure Captions

Fig. 1. Surface reactions during growth of silicon and silicon-germanium alloys: a) chemisorption of silane, germane, and hydrogen; b) creation of new active sites by desorption of hydrogen; and c) reaction of dichlorosilane with the silicon surface, showing processes for the desorption of hydrogen, HCl, and $SiCl_2$.

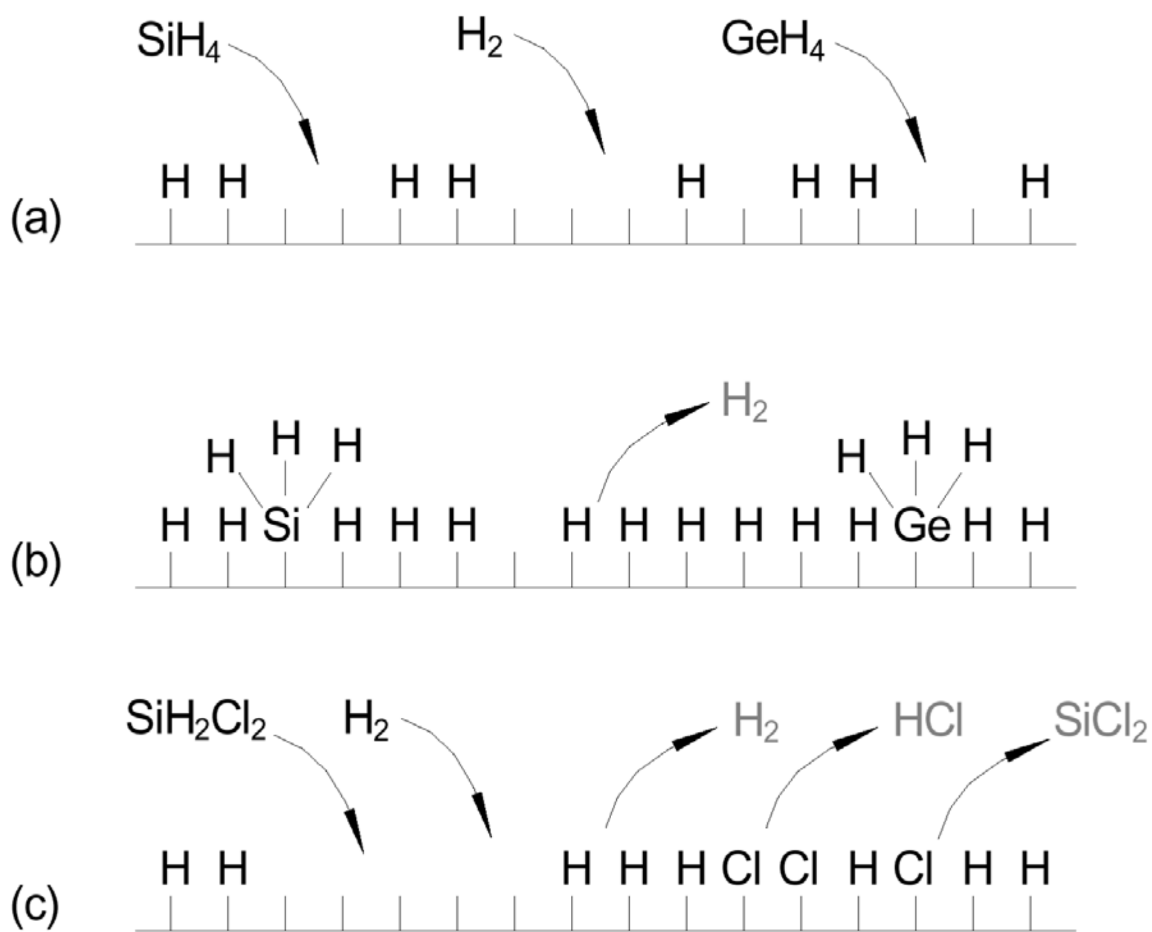
Fig. 2. Collected data showing substitutional carbon concentration as a function of total carbon concentration for growth of $Si_{1-y}C_y$. Various CVD techniques at 550 C with methysilane source for carbon: (●) John et al., single-wafer UHV/CVD with Si_2H_6 silicon source; (▲) Mitchell et al., RTCVD with SiH_4 source, 300 mT; (■) Mitchell et al., RTCVD with SiH_4 source, 1200 mT; and Mocuta and Greve, UHV/CVD with SiH_4 source. MBE: (□) Osten et al., 375 C and 550 C substrate temperatures.

Fig. 3. Growth rate of $Si_{1-y}C_y$ in UHV/CVD as a function of total carbon mole fraction at various temperatures.

Fig. 4. Heterostructure PMOS transistor structure.

Fig. 5. High-resolution X-ray ω-2θ diffraction scans showing relaxation of layers during isochronal (1 hr) anneals: (left) 165 nm thick $Si_{0.91}Ge_{0.09}$; (right) 180 nm thick $Si_{0.888}Ge_{0.11}C_{0.002}$.

Fig. 6. Measured C_{G-SD} (open points) and extracted hole mobility (solid points) for heterostructure p-MOSFET (○,●) and silicon surface-channel MOSFET (□,■) Z/L = 100 μm /50 μm).



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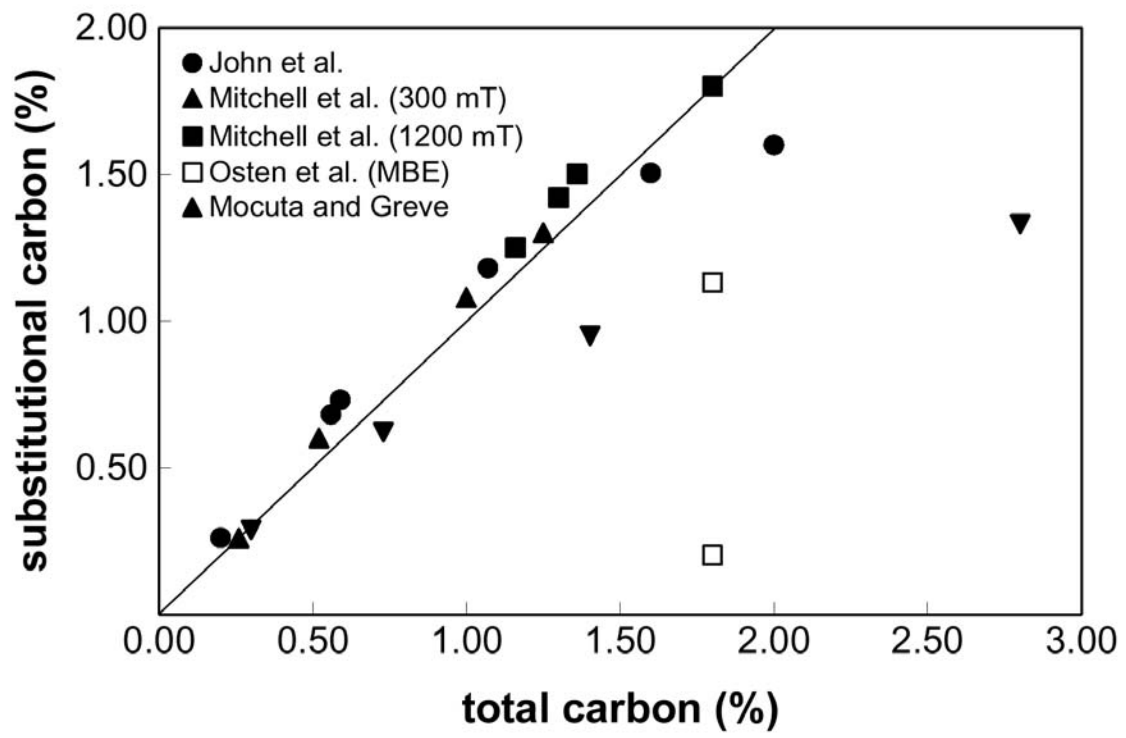

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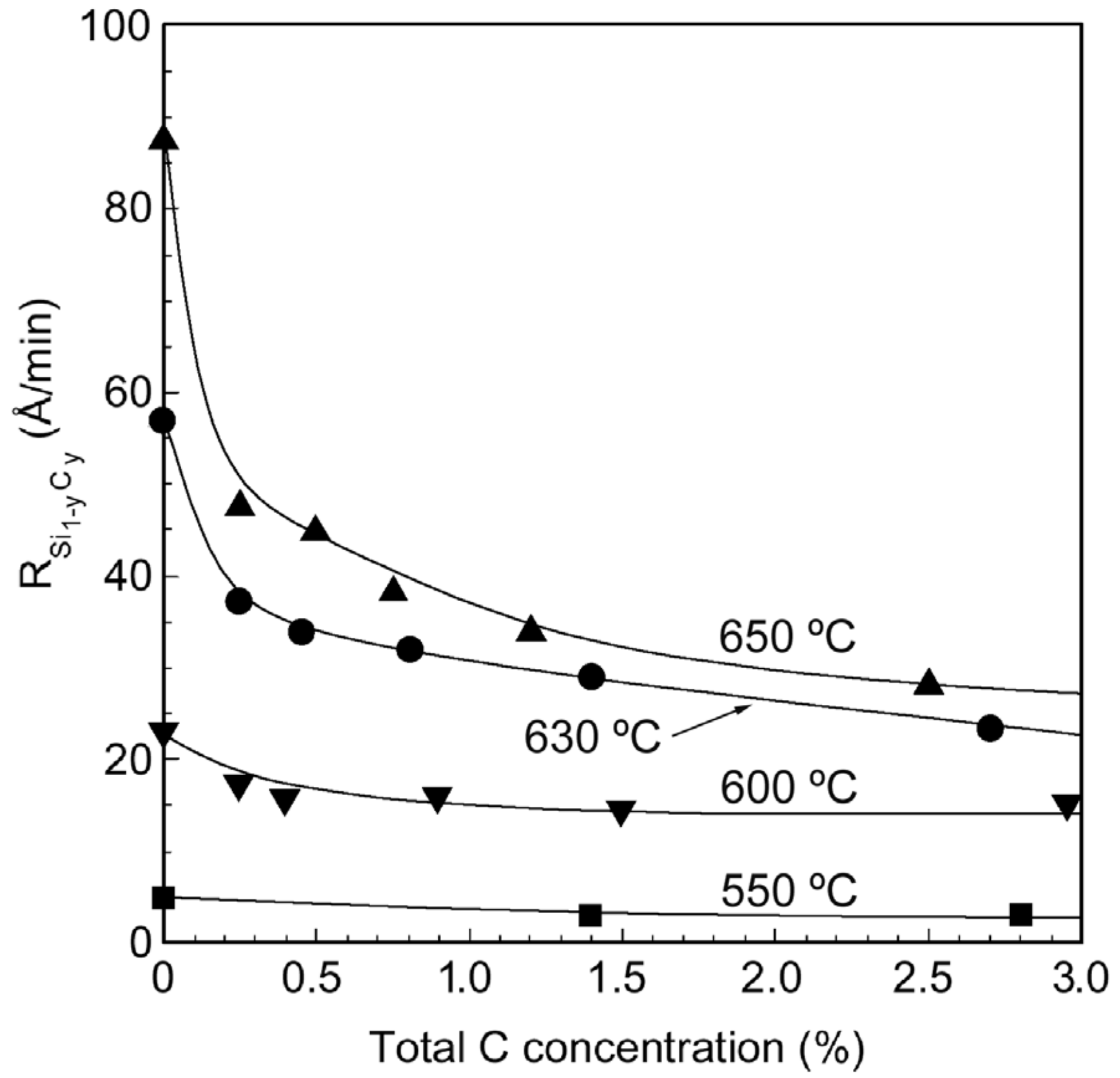

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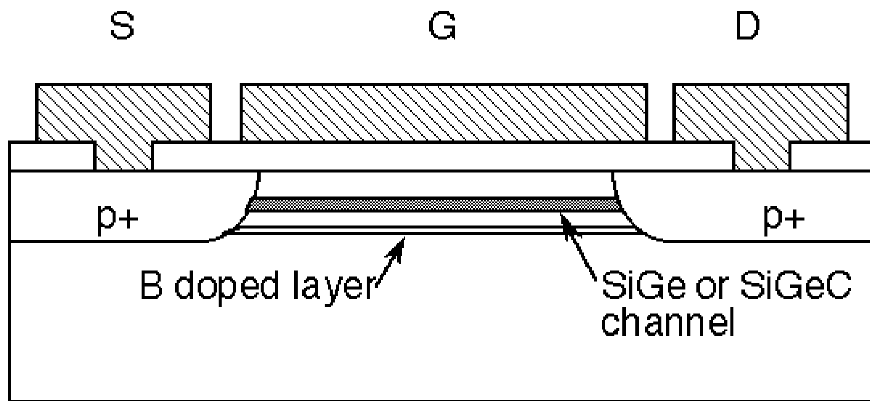

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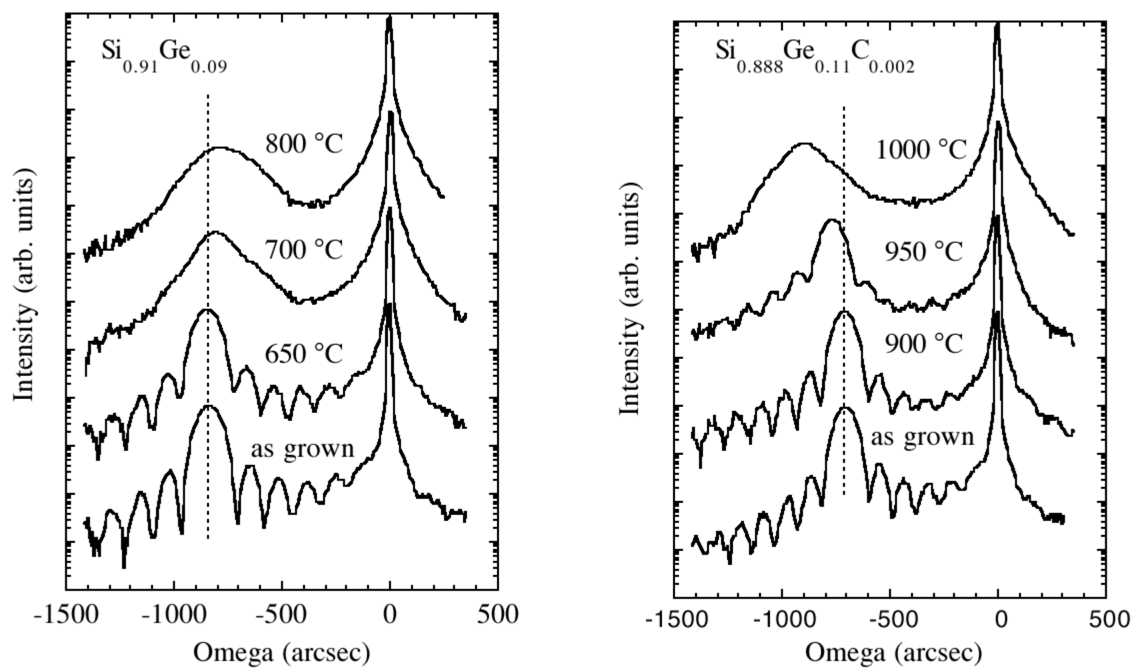

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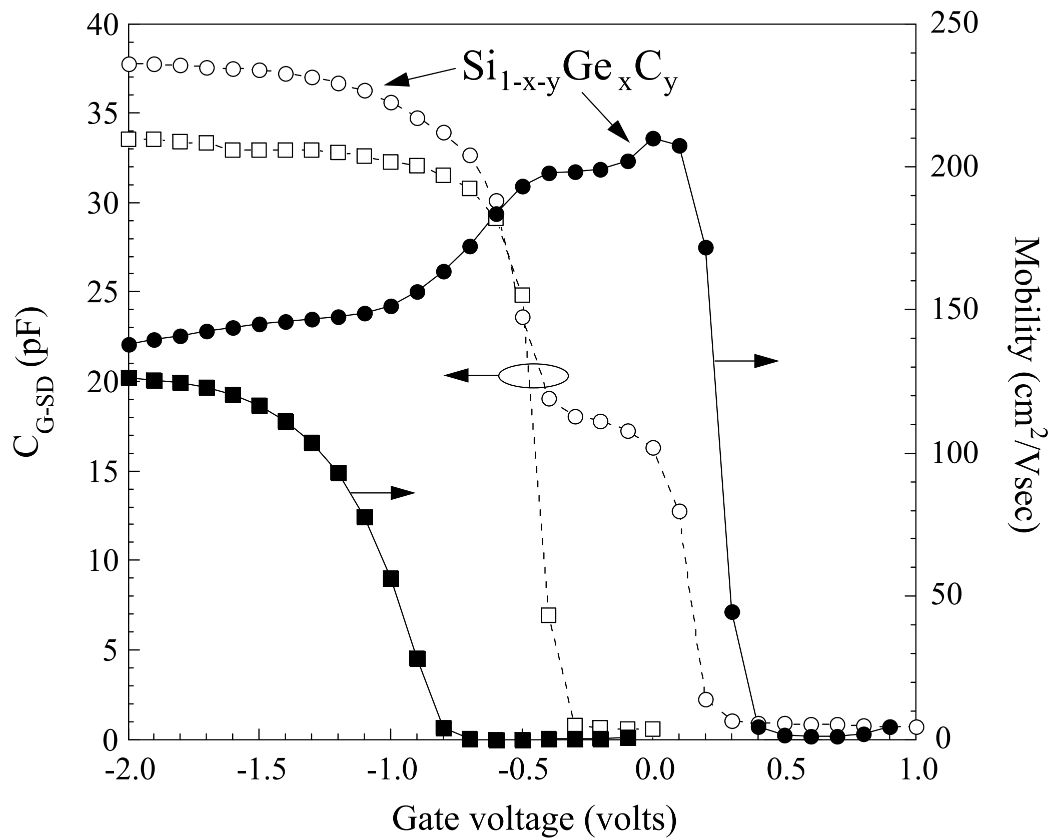

Figure 6.