Arjun Ramesh

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RESEARCH STATEMENT

My research interests encompass **software virtualization** and **debugging** with a strong focus on applications targetting cyber-physical edge systems. With a comprehensive systems background – OS, embedded, compilers, architecture – I am dedicated to enabling robust, usable, and performant software ecosystem design at the edge.

EDUCATION

Carnegie Mellon University — *PhD+MS, Electrical & Computer Engineering* — *GPA: 3.87 | Present*
The University of Texas at Austin — *BS, Electrical & Computer Engineering* — *GPA: 4.00 | Aug 2021*

PUBLICATIONS

Empowering WebAssembly with Thin Kernel Interfaces — *1st Author* — *EuroSys '25*
Unveiling Heisenbugs with Diversified Execution — *1st Author* — *OOPSLA '25*
Silverline: Virtualization and Orchestration of Distributed Systems — *1st Author* — *RTAS '25*
Edge Runtime Prediction using Conformal Matrix Completion — *2nd Author* — *MLSys '25*

WORK EXPERIENCE

IoT Cloud and Edge Integration Intern — *Bosch Research (Pittsburgh, PA)* — *Jun-Aug 2022*
Designed an edge-orchestration framework (Silverline) for real-time industrial automation

GPU Design Verification Intern — *Apple Inc. (Austin, TX)* — *Jun-Aug 2020*
Memory hierarchy testing improvements (speed/coverage); UVM testbenches for M2 Graphics

CPU Design Verification Intern — *Centaur Technology Inc. (Austin, TX)* — *May-Aug 2019*
Memory testing tools for x86/AVX-512 chip and live analysis of CPU exception events

INVITED TALKS

Unveiling CPS Heisenbugs at Scale — *Bosch RDS Tech Colloquium* — *Oct 2024*
Leveraging WebAssembly as a Debugging Target — *Wasm Research Day* — *Jun 2024*
Giving the Cloud an Edge with WebAssembly — *Wasm Research Day (with T. Huang)* — *Oct 2022*

HONORS AND SCHOLARSHIPS

Charles W. and Margaret A. Tolbert Scholarship — High Merit in Engineering — *Fall '20*
Centaur Technology Scholarship — Summer 2019 Internship Package — *Fall '19*
Ray Fisher Memorial Scholarship — High Merit University-Wide — *Fall '19*
UT Austin University Honors — Exemplary GPA (4.0) standing — *Fall '17 - Spr '20*

TECHNICAL PROJECTS

RISC-V CPU Design and ISA Extension — *UT Austin (Capstone)* — *Apr 2021*
Out-of-order RISC-V CPU with custom extensions to accelerate hashsets and graph search — Talk | Github

The JASP Cellular Phone — *UT Austin (445L Class)* — *Dec 2019*
Cellphone designed from scratch with call+text capability; Won 1st place in project showcase — Github

RTOS Design on Bare-Metal Microcontroller — *UT Austin (445M Class)* — *Apr 2020*
Fully featured with process loading, priority scheduling, FAT filesystem, and wireless RPCs — Talk