

Arjun Ramesh

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RESEARCH STATEMENT

I specialize in **virtual machines** and **compilers** with an embedded systems flavor. Driven by a bottom-up approach, my research rethinks the software architecture for resource-constrained edge systems around bytecode virtualization to bring modern programmability and deep-stack observability at minimal performance costs.

EDUCATION

Carnegie Mellon University	<i>PhD+MS, Electrical & Computer Engineering</i>	<i>Jun 2026 (Exp.)</i>
The University of Texas at Austin	<i>BS, Electrical & Computer Engineering</i>	<i>GPA: 4.00 Aug 2021</i>

PUBLICATIONS

Empowering WebAssembly with Thin Kernel Interfaces — 1 st Author	 EuroSys '25
Unveiling Heisenbugs with Diversified Execution — 1 st Author	 Talk  OOPSLA '25
Silverline: Virtualization and Orchestration of Distributed Systems — 1 st Author	 RTAS '25
Edge Runtime Prediction using Conformal Matrix Completion — 2 nd Author	 MLSys '25

SELECTED WORK EXPERIENCE

Programmability Intern — <i>F5 Inc., Office of the CTO (San Jose, CA)</i>	<i>Jun-Aug 2025</i>
Built efficient record/replay feature in Wasmtime compiler to enable time-travel debugging	
IoT Cloud and Edge Integration Intern — <i>Bosch Research (Pittsburgh, PA)</i>	<i>Jun-Aug 2022</i>
Designed an edge-orchestration framework (Silverline) for real-time industrial automation	
GPU Design Verification Intern — <i>Apple Inc. (Austin, TX)</i>	<i>Jun-Aug 2020</i>
Memory hierarchy testing improvements (speed/coverage); UVM testbenches for M2 Graphics	
CPU Design Verification Intern — <i>Centaur Technology Inc. (Austin, TX)</i>	<i>May-Aug 2019</i>
Memory testing tools for x86/AVX-512 chip and live analysis of CPU exception events	

SELECTED INVITED TALKS

Time-Travel Debugging for WebAssembly	Wasm Research Day	<i>Oct '25</i>
Unveiling CPS Heisenbugs at Scale	Bosch RDS Tech Colloquium	<i>Oct '24</i>

SELECTED HONORS

Charles W. and Margaret A. Tolbert Scholarship	High Merit in Engineering	<i>Fall '20</i>
Ray Fisher Memorial Scholarship	High Merit University-Wide	<i>Fall '19</i>

SELECTED TECHNICAL PROJECTS

RISC-V CPU Design and ISA Extension	<i>Apr 2021</i>
Out-of-order RISC-V CPU with custom extensions to accelerate hashsets and graph search	 Talk  GH
The JASP Embedded Cellular Phone	<i>Dec 2019</i>
Cellphone designed from scratch with call+text; Won popular vote in class project showcase	 GH
RTOS Design on Bare-Metal Microcontroller	<i>Apr 2020</i>
Fully featured with process loading, priority scheduling, FAT filesystem, and wireless RPCs	 Talk