WAVELET METHOD FOR HIGH-SPEED CLOCK TREE SIMULATION

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ABSTRACT

In this paper, we propose a fast wavelet collocation algorithm for high-speed clock tree simulation. Taking advantage of the specific structure of clock trees and the superior computational property of wavelets, the proposed algorithm presents the following merits. (1) It can perform both transient simulation and steady-state analysis with arbitrary input. (2) It employs nonlinear buffer model and nonuniform interconnect wire model. (3) It has a low computational complexity $O(N)$ and can deal with considerably large circuits. (4) The proposed wavelet method works in time domain so that the simulation error in time domain can be well-controlled. Numerical experiment results demonstrate the promising features of the proposed algorithm in high-speed clock tree simulations.

1. INTRODUCTION

One of the most challenge tasks involved in multi-GHz microprocessors chip design is to properly construct the clock signal distribution circuits. Under GHz clock rate and deep submicron range, the clock wires present strong transmission line effects and pose strong singularities in signal waveforms. To characterize such signal integrity problem, fast and accurate full waveform simulation tool is inevitably required in the clock routing [1]. During the past several years, analytical formulas [2] or full-waveform simulations [3]-[4] have been developed for interconnect analysis. Due to the simplified model for theoretical analysis, the accuracy of the analytical formulas is not guaranteed to characterize GHz frequency interconnect wires. To tackle with large scale interconnect circuits, order reduction techniques such as moment matching [5]-[6] and TBR [7] have been proposed to represent the linear distributed interconnect network by a reduced-order model. The moment-matching approaches [5]-[6] have achieved spectacular success in solving many practical VLSI interconnect problems. However, the solution obtained is valid only at the neighborhood of the frequency expansion point, and the error cannot be bounded in a wide frequency range. The truncated balanced realizations TBR [7] have a well-defined error bound in both frequency and time domain. Unfortunately, the computational complexity is $O(N^3)$, which limits their application in large circuits.

Recently, the wavelet theory has been developed for high-speed circuit simulations [8]-[9]. However, the complexity of FWCM in [8] is also $O(N^3)$. Due to the compact support and $O(h^4)$ convergence rate of B-spline wavelets in [8]-[9], we expect that the wavelet method will be very powerful in dealing with the strong singularities in GHz clock signals and achieving uniform error distribution in time domain. In this paper, we aim to develop a specific wavelet simulation algorithm for clock tree simulation, which has linear complexity to effectively handle large scale distributed circuits and in the meantime guarantee the accuracy of the simulation results in the whole time region. Moreover, we employ the nonuniformly distributed transmission line model and nonlinear buffer model in the proposed algorithm to further improve the simulation accuracy.

The rest of this paper is organized as follows. We develop the wavelet algorithm for simulating single interconnect wire in Section 2 and extend the proposed algorithm to high-speed clock tree simulations in Section 3. The complexity analysis of the proposed algorithm is presented in Section 4. Experiment results and conclusions are given in Section 5 and Section 6.

2. WAVELET ALGORITHM FOR SINGLE WIRE SIMULATION

In this section, we first propose the wavelet models for the *RLC* element block and the whole interconnect wire. Then we present the nonlinear buffer model and illustrate how to combine the wavelet models with the nonlinear buffers to simulate the single interconnect wire.

2.1. Wavelet model for element *RLC* block

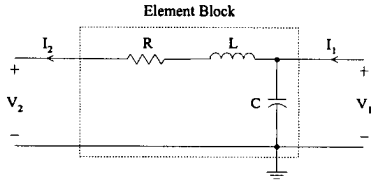

Fig. 1. Element *RLC* block in interconnect wire

Shown in Fig. 1 is the RLC element block in interconnect wire. In time domain, the relation between the input voltage/current (V_1, I_1) and output voltage/current (V_2, I_2) is

$$\begin{bmatrix} V_2(t) \\ I_2(t) \end{bmatrix} = \begin{bmatrix} LC\frac{d^2}{dt^2} + RC\frac{d}{dt} + 1 & -\left(L\frac{d}{dt} + R\right) \\ -C\frac{d}{dt} & 1 \end{bmatrix} \cdot \begin{bmatrix} V_1(t) \\ I_1(t) \end{bmatrix} \quad (1)$$

we expand the input-output variables by wavelets, i.e.

$$\begin{aligned} V_1(t) &= Q_{V1} \cdot W(t) \quad V_2(t) = Q_{V2} \cdot W(t) \\ I_1(t) &= Q_{I1} \cdot W(t) \quad I_2(t) = Q_{I2} \cdot W(t) \end{aligned} \quad (2)$$

where $W(t) = [W_1(t) \;\; W_2(t) \;\; \cdots \;\; W_M(t)]^T$ are wavelet basis functions, $Q_{V1}, Q_{I1}, Q_{V2}, Q_{I2} \in R^{1\times M}$ are coefficient vectors, and M is the total number of basis functions. Substituting (2) into (1), we get

$$\begin{bmatrix} Q_{V2}W(t) \\ Q_{I2}W(t) \end{bmatrix} = \begin{bmatrix} LC\frac{d^2}{dt^2} + RC\frac{d}{dt} + 1 & -\left(L\frac{d}{dt} + R\right) \\ -C\frac{d}{dt} & 1 \end{bmatrix} \cdot \begin{bmatrix} Q_{V1}W(t) \\ Q_{I1}W(t) \end{bmatrix} \quad (3)$$

In order to transfer the time domain specification (3) into wavelet domain, we discretizate equation (3) at some interior collocation points $\{t_1, t_2, \cdots, t_M\}$ [8]-[9] and derive the wavelet model in equation (4).

$$Q_{V2}\cdot W_C=[Q_{V1}\quad Q_{I1}]\cdot\begin{bmatrix}LC\hat{D}_2+RC\hat{D}_1+\hat{I}\\-(L\hat{D}_1+R)\end{bmatrix}\cdot W_C \qquad (4)$$

$$Q_{I2}\cdot W_C=[Q_{V1}\quad Q_{I1}]\cdot\begin{bmatrix}-C\hat{D}_1\\\hat{I}\end{bmatrix}\cdot W_C$$

where $\hat{I}\in R^{M\times M}$ is the identity matrix, $W_C\in R^{M\times M}$ in equation (5) includes the wavelet basis function values at different collocation points, and $\hat{D}_1,\hat{D}_2\in R^{M\times M}$ in equation (6) and (7) are respectively the first-order and second-order derivative matrix.

$$W_C=\begin{bmatrix}W_1(t_1) & W_1(t_2) & \cdots & W_1(t_M)\\ W_2(t_1) & W_2(t_2) & \cdots & W_2(t_M)\\ \vdots & \vdots & \vdots & \vdots\\ W_M(t_1) & W_M(t_2) & \cdots & W_M(t_M)\end{bmatrix} \qquad (5)$$

$$\hat{D}_1=\begin{bmatrix}\frac{d}{dt}W_1(t_1) & \frac{d}{dt}W_1(t_2) & \cdots & \frac{d}{dt}W_1(t_M)\\ \frac{d}{dt}W_2(t_1) & \frac{d}{dt}W_2(t_2) & \cdots & \frac{d}{dt}W_2(t_M)\\ \vdots & \vdots & \vdots & \vdots\\ \frac{d}{dt}W_M(t_1) & \frac{d}{dt}W_M(t_2) & \cdots & \frac{d}{dt}W_M(t_M)\end{bmatrix}\cdot W_C^{-1} \qquad (6)$$

$$\hat{D}_2=\begin{bmatrix}\frac{d^2}{dt^2}W_1(t_1) & \frac{d^2}{dt^2}W_1(t_2) & \cdots & \frac{d^2}{dt^2}W_1(t_M)\\ \frac{d^2}{dt^2}W_2(t_1) & \frac{d^2}{dt^2}W_2(t_2) & \cdots & \frac{d^2}{dt^2}W_2(t_M)\\ \vdots & \vdots & \vdots & \vdots\\ \frac{d^2}{dt^2}W_M(t_1) & \frac{d^2}{dt^2}W_M(t_2) & \cdots & \frac{d^2}{dt^2}W_M(t_M)\end{bmatrix}\cdot W_C^{-1} \qquad (7)$$

Note that the initial conditions haven't been included in equation (4). Actually, (4) may lead to different solutions if different initial conditions are considered.

2.1.1. Solution of Transient Response

In this subsection, we will derive the transient response of the interconnect wire. Without loss of generality, we assume the initial conditions for L and C (Fig. 1) are zeros so that the input-output variables V_1, I_1, V_2 and I_2 satisfy equation (8).

$$\begin{aligned}V_2&=-L\frac{dI_2}{dt}\quad(t=0)\\ I_2&=0\quad(t=0)\end{aligned} \qquad (8)$$

Combining equation (4) and (8), we may obtain the following relation.

$$[Q_{V2}\quad Q_{I2}]=[Q_{V1}\quad Q_{I1}]\cdot P=[Q_{V1}\quad Q_{I1}]\cdot\begin{bmatrix}P^A & P^B\\ P^C & P^D\end{bmatrix} \qquad (9)$$

where $P^A,P^B,P^C,P^D\in R^{M\times M}$ are sub-matrixes in P

$$\begin{aligned}P^A&=LC\hat{D}_1\hat{T}_{T1}\hat{D}_1\hat{T}_{T2}+LC\hat{D}_2\hat{T}_{T1}+RC\hat{D}_1\hat{T}_{T1}+\hat{T}_{T1}\\ P^B&=-C\hat{D}_1\hat{T}_{T1}\\ P^C&=-L\hat{T}_{T1}\hat{D}_1\hat{T}_{T2}-L\hat{D}_1\hat{T}_{T1}-R\hat{T}_{T1}\\ P^D&=\hat{T}_{T1}\end{aligned} \qquad (10)$$

$$\begin{aligned}\hat{T}_{T1}&=W_CW_C^T\left[W(0)W^T(0)+W_CW_C^T\right]^{-1}\\ \hat{T}_{T2}&=W(0)W^T(0)\left[W(0)W^T(0)+W_CW_C^T\right]^{-1}\end{aligned} \qquad (11)$$

where $W(0)$ includes the wavelet basis function values at $t=0$, and superscript T denotes the operation of transpose.

2.1.2. Solution of Steady-State Response

To analyze the steady-state response of the interconnection wire, the output variables V_2 and I_2 are forced to satisfy the two-point boundary constraints,

$$\begin{aligned}V_2(t=0)&=V_2(t=T_{Period})\\ I_2(t=0)&=I_2(t=T_{Period})\end{aligned} \qquad (12)$$

where T_{Period} is the response period determined by the input excitations. Regarding equation (4) and (12), we may obtain the similar input-output relation as equation (9) except that the matrix P^A, P^B, P^C and P^D are given by

$$\begin{aligned}P^A&=LC\hat{D}_2\hat{T}_S+RC\hat{D}_1\hat{T}_S+\hat{T}_S;\quad P^B=-C\hat{D}_1\hat{T}_S\\ P^C&=-L\hat{D}_1\hat{T}_S-R\hat{T}_S;\quad P^D=\hat{T}_S\end{aligned} \qquad (13)$$

where

$$\hat{T}_S=W_CW_C^T\cdot\left[W(0)-W(T_{Period})\right]\cdot\left[W(0)-W(T_{Period})\right]^T+W_CW_C^T\Big]^{-1} \qquad (14)$$

In summary, the above analysis indicates that the input coefficient vectors $[Q_{V1}\quad Q_{I1}]$ can be mapped to the outputs $[Q_{V2}\quad Q_{I2}]$ by a linear transform P. Either transient response or steady-state response can be obtained by employing different transform matrix P.

2.2. Wavelet model for interconnect wire

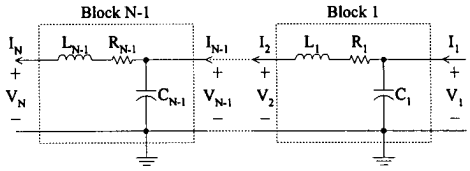

Fig. 2. Model for interconnect wire

Shown in Fig. 2 is the nonuniform transmission line model cascaded by N RLC element blocks, each of which may have different R, L, C values. Based on the results in Section 2.1, we can find out the transform matrix P^i for each element block i. Then the wavelet domain expression for the input-output relation of the interconnect wire is given by

$$\begin{aligned}[Q_{VN}\quad Q_{IN}]&=[Q_{V1}\quad Q_{I1}]\cdot P^1\cdot P^2\cdot\cdots\cdot P^{N-1}\\ &=[Q_{V1}\quad Q_{I1}]\cdot P_{N-1}\end{aligned} \qquad (15)$$

where Q_{VN} and Q_{IN} are wavelet coefficient vectors for representing $V_N(t)$ and $I_N(t)$ (Fig. 2) respectively, and $P_{N-1}=P^1\cdot P^2\cdot\cdots\cdot P^{N-1}$. Note that the transform matrixes $P^1,P^2,\cdots,P^{N-1}$ are different from each other for nonuniform interconnect line and shall be constant if uniform line is studied.

2.3. Dealing with nonlinear buffers

Fig. 3. Interconnect wire with excitation and load buffer

In this subsection, we will simulate the interconnect wire with one excitation buffer and one load buffer, as shown in Fig. 3. The excitation buffer is modeled as a nonlinear voltage source

$$V_N=f(I_N,V_{in}) \qquad (16)$$

where V_{in} is the input voltage of the excitation buffer, and V_N and I_N are its output voltage and current respectively. In the meantime, the load buffer is simplified as a linear capacitance C_L. Therefore, at the load point, the voltage V_1 and the current I_1 shall satisfy the boundary constraint

$$I_1=-C_L\cdot\frac{dV_1}{dt} \qquad (17)$$

or equivalently in wavelet domain, the wavelet coefficients shall

satisfy

$$Q_{I1} = -C_L \cdot Q_{V1} \cdot \hat{D}_1 \tag{18}$$

Substituting (18) into (15), we can express coefficient vectors Q_{VN} and Q_{IN} by Q_{V1}

$$\begin{aligned} Q_{VN} &= Q_{V1} \cdot \left(P_{N-1}^{A} - C_L \cdot \hat{D}_1 \cdot P_{N-1}^{C}\right) \\ Q_{IN} &= Q_{V1} \cdot \left(P_{N-1}^{B} - C_L \cdot \hat{D}_1 \cdot P_{N-1}^{D}\right) \end{aligned} \tag{19}$$

where $P_{N-1}^{A}, P_{N-1}^{B}, P_{N-1}^{C}, P_{N-1}^{D} \in R^{M \times M}$ are sub-matrixes in P_{N-1}

$$P_{N-1} = \begin{bmatrix} P_{N-1}^{A} & P_{N-1}^{B} \\ P_{N-1}^{C} & P_{N-1}^{D} \end{bmatrix} \tag{20}$$

On the other hand, at the excitation point, we have

$$\begin{aligned} &Q_{VN} \cdot [W(t_1) \ \cdots \ W(t_M)] = \\ &\quad [f(Q_{IN} W(t_1), V_{in}(t_1)) \ \cdots \ f(Q_{IN} W(t_M), V_{in}(t_M))] \end{aligned} \tag{21}$$

where $\{t_1, t_2, \cdots, t_M\}$ are interior collocation points. Regarding equation (19), we formulate (21) as a nonlinear equation in terms of Q_{V1}

$$\begin{aligned} &Q_{V1}\left(P_{N-1}^{A} - C_L \hat{D}_1 P_{N-1}^{C}\right) \cdot [W(t_1) \ \cdots \ W(t_M)] = \\ &\quad \left[f\left[Q_{V1} \cdot \left(P_{N-1}^{B} - C_L \hat{D}_1 P_{N-1}^{D}\right) \cdot W(t_1), V_{in}(t_1)\right] \ \cdots \right. \\ &\quad \left. f\left[Q_{V1} \cdot \left(P_{N-1}^{B} - C_L \hat{D}_1 P_{N-1}^{D}\right) \cdot W(t_M), V_{in}(t_M)\right]\right] \end{aligned} \tag{22}$$

In addition, the circuit response V_1 shall satisfy the following initial conditions

$$\begin{aligned} &Q_{V1} W(0) = 0 && (\textit{for transient response}) \\ &Q_{V1} W(0) = Q_{V1} W(T_{Period}) && (\textit{for steady-state response}) \end{aligned} \tag{23}$$

The above nonlinear equations (22) and (23) can be solved if the optimization algorithm, such as the Levenberg-Marquardt method [10], is applied. Consequently, the transient/steady-state response of the interconnect wire is obtained.

3. WAVELET ALGORITHM FOR CLOCK TREE SIMULATION

In this section, we extend the developed algorithm in Section 2 to high-speed clock tree simulation.

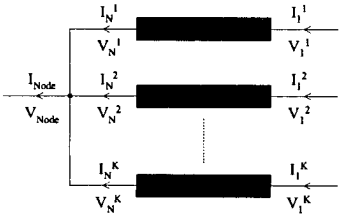

Fig. 4. Typical topology in clock tree

The difference between a single interconnect line and the clock tree is that in clock tree two or more branches will combine into one at their father node, as shown in Fig. 4. We adopt a bottom-up approach for clock tree simulation. We start analysis at the bottom of the tree (the leaf nodes), then go to the intermediate nodes, and finally deal with the root node.

At the leaf nodes, if K branches connect with each other at their father node, as depicted in Fig. 4, we have

$$\begin{aligned} V_{Node} &= V_N^1 = V_N^2 = \cdots = V_N^K \\ I_{Node} &= I_N^1 + I_N^2 + \cdots + I_N^K \end{aligned} \tag{24}$$

where V_N^i and I_N^i $(i = 1,2,\cdots,K)$ are respectively the voltage and the current at the terminal of ith downstream branch (Fig. 4). V_{Node} and I_{Node} are respectively the voltage and the current of the upstream branch (Fig. 4). Based on equation (24), the wavelet coefficients shall satisfy

$$\begin{aligned} Q_{VNode} &= Q_{VN}^1 = Q_{VN}^2 = \cdots = Q_{VN}^K \\ Q_{INode} &= Q_{IN}^1 + Q_{IN}^2 + \cdots + Q_{IN}^K \end{aligned} \tag{25}$$

where Q_{VN}^i and Q_{IN}^i $(i = 1,2,\cdots,K)$ are wavelet coefficient vectors for representing $V_N^i(t)$ and $I_N^i(t)$ respectively. Q_{VNode} and Q_{INode} are wavelet coefficient vectors for representing V_{Node} and I_{Node} respectively. Regarding equation (19), the coefficient vector $\begin{bmatrix} Q_{VN}^i & Q_{IN}^i \end{bmatrix}$ can be expressed as a linear transform of Q_{V1}^i, i.e.

$$\begin{aligned} Q_{VN}^i &= Q_{V1}^i \cdot \left(P_{N-1}^{Ai} - C_L^i \cdot \hat{D} \cdot P_{N-1}^{Ci}\right) \\ Q_{IN}^i &= Q_{V1}^i \cdot \left(P_{N-1}^{Bi} - C_L^i \cdot \hat{D} \cdot P_{N-1}^{Di}\right) \end{aligned} \tag{26}$$

With equation (25) and (26), we can obtain

$$\begin{aligned} Q_{VNode} &= Q_{V1}^i \cdot P_{Node}^{Ai} \quad (i = 1,2,\cdots,K) \\ Q_{INode} &= Q_{V1}^i \cdot P_{Node}^{Bi} \quad (i = 1,2,\cdots,K) \end{aligned} \tag{27}$$

where

$$\begin{aligned} P_{Node}^{Ai} &= \left(P_{N-1}^{Ai} - C_L^i \hat{D} P_{N-1}^{Ci}\right) \\ P_{Node}^{Bi} &= \left(P_{N-1}^{Ai} - C_L^i \hat{D} P_{N-1}^{Ci}\right) \cdot \sum_{j=1}^{K} \left[\left(P_{N-1}^{Aj} - C_L^j \hat{D} P_{N-1}^{Cj}\right)^{-1} \cdot \right. \\ &\quad \left. \left(P_{N-1}^{Bj} - C_L^j \hat{D} P_{N-1}^{Dj}\right)\right] \end{aligned} \tag{28}$$

Equation (28) indicates that we can obtain an explicit formula to express Q_{VNode} and Q_{INode} only by one coefficient vector $Q_{V1}^i, \forall i \in \{1,2,\cdots,K\}$. Repeating the same operation for several times, we can get a set of linear equations that only include the root node and the leaf nodes

$$\begin{aligned} Q_{VRoot} &= Q_{V1}^i \cdot P_{Root}^{Ai} \quad (i = 1,2,\cdots,K) \\ Q_{IRoot} &= Q_{V1}^i \cdot P_{Root}^{Bi} \quad (i = 1,2,\cdots,K) \end{aligned} \tag{29}$$

Finally, the excitation buffer at the root node is modeled by a nonlinear source (16), and the circuit response at both root node and the leaf nodes can be obtained by applying the algorithm in Section 2.3.

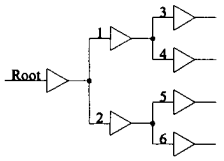

Fig. 5. Clock tree with more than one nonlinear excitation buffers

If there are more than one nonlinear excitation buffers in clock tree, as shown in Fig. 5, we can simulate the tree in a pipeline scheme. Taking the clock tree in Fig. 5 for example, we first find the response voltage at node 1 and node 2 using the proposed method. Then, repeat the same simulation procedure to find the circuit responses at node 3, 4, 5, 6 and other downstream nodes until the leaf nodes are reached. In such a strategy, we can obtain all clock signal waveforms in the clock tree circuit.

4. COMPLEXITY ANALYSIS

The complexity for constructing the formula (15) is $O(N)$, where N is the number of cascaded element blocks in a single interconnect wire. The computation cost of the operations in Section 2.1 and 2.3 only depends on M (the number of collocation points), which is not related to the circuit size.

Therefore, the overall computational complexity for simulating single interconnect wire is $O(N)$. For clock tree simulation, the computation cost of the additional operations performed at each branching vertex depends linearly on the number of the branching vertices (Section 3). Hence, the overall computational complexity of the proposed algorithm for clock tree simulation remains $O(N)$, where N refers to the circuit size, i.e. the total number of element blocks and branching vertices.

5. NUMERICAL EXPERIMENTS

In this section, several circuit examples are examined on a Pentium III 550 computer to demonstrate the accuracy and computational efficiency of the proposed method in high-speed clock tree simulations.

4.1 Transient simulations

Table 1. Circuit sizes and simulation errors of 8 clock trees.

Circuit No.	Circuit Size	Simulation Error
1	51	1.480383×10^{-2}
2	148	1.165245×10^{-2}
3	342	8.948777×10^{-3}
4	730	7.379149×10^{-3}
5	1506	2.275622×10^{-2}
6	3058	8.131610×10^{-3}
7	6162	8.342300×10^{-3}
8	12370	5.797106×10^{-3}

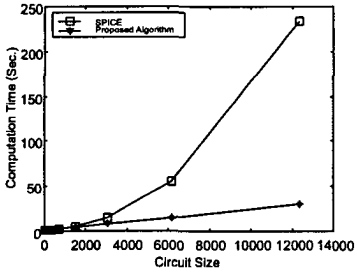

Fig. 6 Computation time for different simulation methods

We simulate the step response of eight clock tree circuits generated by [1] and obtained the simulation errors of the proposed algorithm compared with SPICE in Table 1. It is shown that the relative errors are all within 2.5%. Fig. 6 depicts the computation time spent by different circuit sizes (numbers of components) for different simulation methods. Note that the computation time of the proposed wavelet method increases linearly with the circuit size and the maximum speed-up (No. 8 clock tree circuit) is about one order compared with SPICE.

4.2 Steady-state simulations

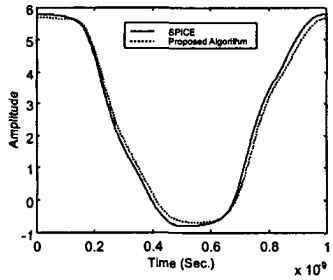

Fig.7 Steady-state response of clock tree circuit

A clock tree circuit with 1037 components with operation frequency of 1GHz is employed for steady-state simulation. Fig. 7 depicts the circuit response obtained by SPICE and the wavelet method. The state equations shall be integrated by SPICE for quite a long time until the transients die out. The relative simulation error in Fig. 7 is 5.65%.

6. CONCLUSIONS

In this paper, we propose a fast wavelet collocation algorithm for high-speed clock tree simulation. The wavelet method can efficiently deal with time domain singularities in GHz clock signal waveforms so that the simulation error in time domain can be well-controlled. The proposed algorithm can perform both transient simulation and steady-state analysis with arbitrary input. The algorithm takes into account the nonlinear buffer model, inductance L and nonuniform interconnect wire. The algorithm has a low $O(N)$ computational complexity and can deal with considerably large circuits. The proposed method is very promising to be embedded in some clock tree routing tools for designing high-performance clock signal distribution networks.

In future work, we'll compare this method with traditional model order reduction methods such as PVL and others. Also, more accurate model for the buffer is under research, which will lead to more precise simulation result.

7. ACKNOWLEDGMENTS

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