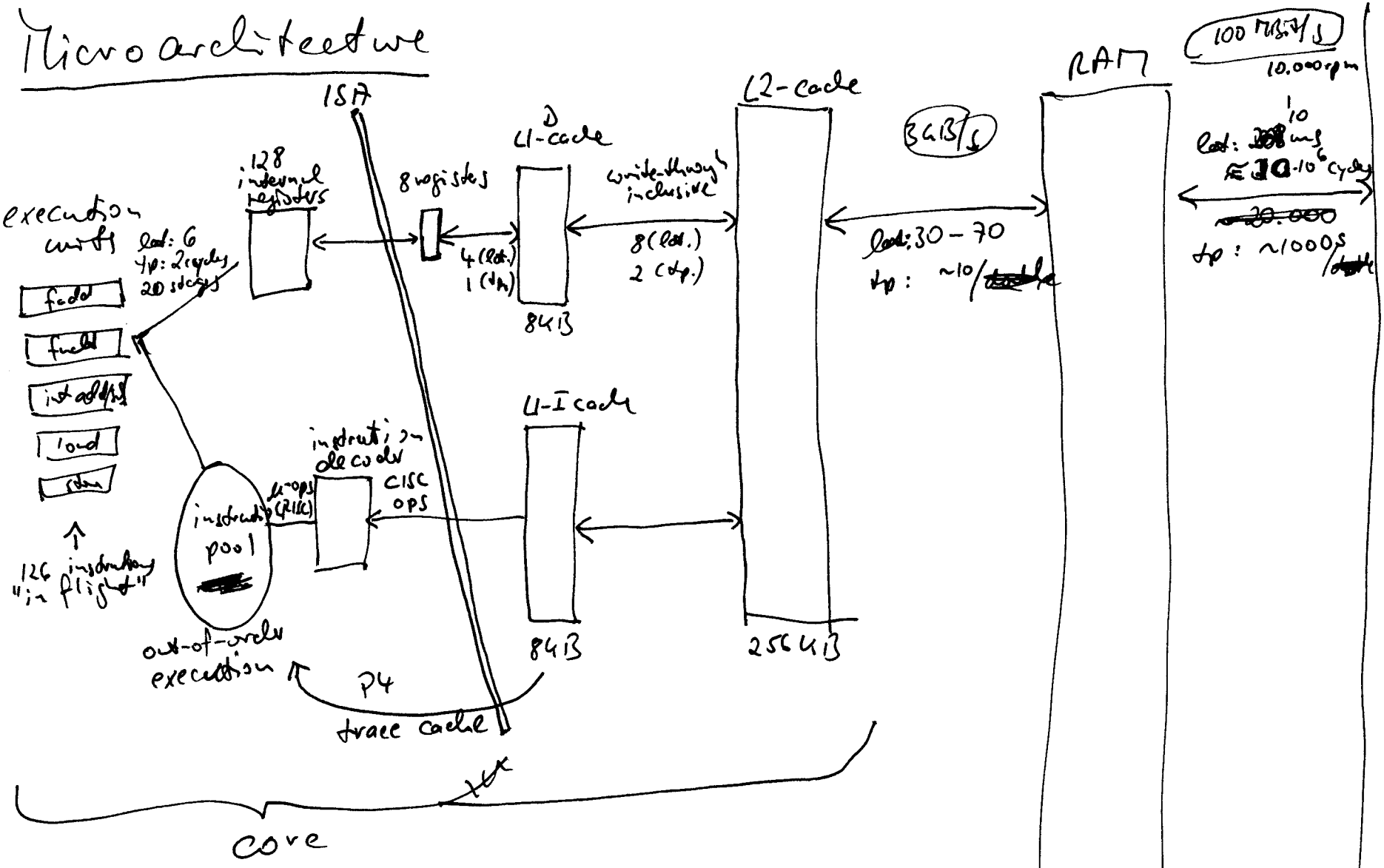
Micro architecture



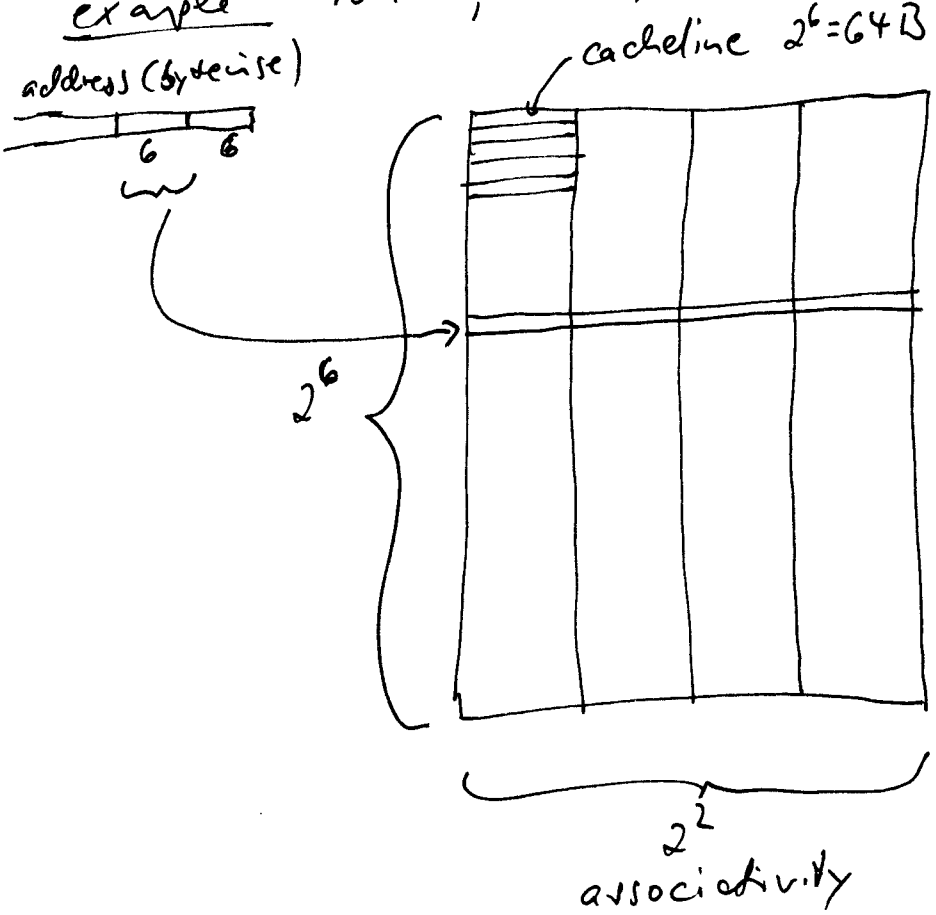
show:

- link to cores
- link to micro architectures
- exec. units picture + peak performance P4

Note: throughput (tp) is given in a nonstandard way, namely cycles/double

Cache structure 2^{14}B

example 16kB, 4-way set associative cache



LRU replacement

- explain cache misses (compulsory, capacity, conflict)
- accessing a vector in unit stride
- " in 2-power stride
- 1 datum → 8 bought in cache, $\frac{1}{8}$ CM's for vector length n
- accessing a 2D-array
  - C
  - Fortran