Multi-Chip Module Smart Substrate Systems

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Abstract

This paper proposes a Smart Substrate Multi-chip Module system implementation strategy. This strategy enables incremental test of all system components and therefore provides an alternative solution to the "Known Good Die" MCM problem. The presentation is focused on a simple microcontroller emulator - designed and fabricated to study test logic needed as a key component of Smart Substrate methodology

1. INTRODUCTION

The Multi-chip Module (**MCM**) concept has as many enthusiastic supporters as opponents [HaW92, Si92, FrE93], and all of them have investigated this relatively old packaging idea from various perspectives. Results obtained by both "camps" indicate low volume, high reliability and top system performance as the most important potentials of the MCM technologies. Both sides of the MCM debate, however, agree that the cost of MCM's may be high - in many cases higher than the cost of equivalent traditional solutions. Among expensive differences between MCM systems and equivalent traditional systems is a need for "known good die," i.e., a need for extensive testing of all MCM components executed prior to module assembly. This need is especially critical in the case of MCM systems with more than a few components. Such systems may yield very poorly unless each system component is tested in a manner ensuring - with a high level of confidence - its proper functionality. A implementation strategy for MCM Smart Substrate System (MCM S^3), has been developed to address these economic issues. The goal of this paper is to describe this methodology and to present a prototype MCM S^3 system which has been manufactured under a co-operative project between Carnegie Mellon University and National Semiconductor Corporation.

2. NEEDED ATTRIBUTES OF MODERN SYSTEM INTEGRATION STRATEGIES

In last couple of years traditional system integration strategies have proven inadequate - especially when power, interconnect speed or system volume have been critical in achieving desired system specs. Consequently, system integration issues have been discussed with growing intensity. The outcome of these discussions can be summarized in form of the following list of observations:

1. A higher level of system integration is an inevitable necessity for a large portion of the systems designed and to be designed in the 90's.
2. There are two major options for increasing system level integration: (a) large area monolithic systems, accomplished by both the decrease of minimum feature size and increase of a die size, or (b) hybrids. Within the family of hybrids there exist a number of options which include MCMs and advanced PCB with IC chips directly mounted on the board.
3. Cost analyses indicate [Ma92] that large area ULSI chips are least likely to be winners. The most likely solution will be (a) inexpensive MCMs (for the high performance end of the market) and (b) some combination of packaging and PCB technology (for the high volume, low cost, oriented segment of the market).
4. Momentum developed in last twenty years and inherent intellectual inertia will still support traditional (i.e. using smaller feature size) technologies in both the IC and system integration arenas. However, the mainstream system integration strategy will be decided by many small/medium system houses which will not be able to afford submicron monolithic solutions (requiring billion dollar range investments).

Hence, to correctly assess possible future needs and the direction of the evolution of system integration one should focus on characteristics of integration strategies important to smaller system houses. Among these desired characteristics are:

1. The ability to provide performance approaching performance of monolithic systems (This is necessary to compete with manufacturers with access to greater financial resources and are able to invest in brute-force-smaller-feature-size solutions).
2. The ability to maximize utilization of existing but still sound and underutilized manufacturing facilities (to minimize cost).
3. Ease of product customization or personalization and/or in-field

programmability. This is necessary to take advantage of market niches not accessible to producers involved in high volume operations.

4. Manufacturing efficiency achieved by producing costly components in high a volume.
5. Second source supplier flexibility (i.e. an ability to easily incorporate components fabricated and designed by independent silicon vendors.)

The strategy possessing all these characteristics is likely to dominate the future of the system integration arena. The key and the most difficult element of such a strategy is the incorporation of all the above characteristics in a single implementation paradigm. The main purpose of this paper is to propose such a strategy.

3. MULTI-CHIP MODULES

One of the well known and frequently discussed possibilities in addressing the above listed requirements is provided by the Multi-chip Module concept. The advantages of this concept do not need to be recalled here. There are , however, some disadvantages of the MCM integration strategies which need to be considered in this paper. They are due to the fact that the traditional MCM arena is strongly influenced by "packaging" perspective, experience and technology. Consequently, traditional MCM's use passive substrates of various kinds. The passive nature of the substrate on one hand enables efficient interconnect and low cost system integration solutions. On the other hand it imposes a number of limitations which, in certain cases, may outweigh benefits produced by the low cost of the passive substrate. The remainder of this section analyzes choice of the MCM substrate from an overall system/implementation perspective in order to set a stage for the implementation strategy postulated in this paper.

3.1 Multi-chip Modules System Yield Problem

The passive nature of the substrate in a typical MCM is responsible for the MCM system yield problem. It has two main aspects. The first is the "incompletely tested die problem" resulting from the fact that the bare IC's used as components of MCM's do not undergo final packaged-chip testing before assembly. Because the electrical environment during wafer probe testing is very difficult for certain speed-related tests, very often bare dies used in MCM assembly are only partially tested (no at-speed test). This way faulty chips may be assembled into the MCM system, resulting in unacceptably low module yield. Second is the "isolation problem" resulting from the physical inaccessibility of the I/O pins

of the component dies after mounting on the substrate. The reduced observability and controllability of the components makes it difficult or impossible to isolate chips for testing and diagnosis once they are mounted on the substrate. The resulting inability to identify the faulty component(s) in a non-functioning module makes it very difficult to use rework (replacement of faulty dies) as a means of increasing the overall module yield.

3.2 Multi-chip Modules with Active Substrate

Observe now that one can view a design of MCMs from a system standpoint and treat the substrate as an active component of the system [Md84, Te89, Ma92]. In such a case, system integration strategy can be seen as a " 2.5 - dimensional " (2.5 - D) integration process in which active system elements are bonded one to another and all of them perform functions which are determined by a system partitioning strategy.

The main aspects of the 2.5 D system integration strategy can be illustrated by an "artist's vision" shown in Fig. 1. The system shown in this figure is assembled on a large-area active substrate i.e. substrate in which one forms MOS or bipolar transistors. The technology of such a substrate is optimized for low cost, power and speed of the interconnect. The performance-critical components of the system are fabricated separately using high volume, high performance oriented fablines. Then they are attached to the active substrate with, for instance, flip-chip technology.

Hence, the key difference between the traditional MCM strategy and 2.5-D integration scheme is in the application of the active substrate. These substrates could be designed such that:

1. Power hungry system elements will be allocated in the substrate. (It is possible to design a system with vast majority of I-O buffers in the active substrate which is much better than flipped system components as far as power dissipation is concerned.)
2. Substrate will include extensive design for testing (DFT) provisions. Boundary scans for the testability of system's components as well as circuitry for substrate self-testing (possible before and after assembly of system's components) could be provided. One could also consider structures which increase system observability through application of extra testing pads or similar solutions.
3. Substrate will be a universal frame for a variety of "specialized" systems (e.g. systems using one vs. three floating point units or variety of memory capacity configurations).

There are a number of positive characteristics of a system using the 2.5 D

implementation strategy. First of all it would provide an opportunity for cost minimization and flexibility in addressing market needs. Note that with this scheme and appropriate design one can prefabricate (and purchase) the main components of the system which can then be customized or even personalized in the assembly. For instance, in the system shown in Fig. 1 one could provide a customer with the task optimized instruction sets (by appropriate design of ROMs) or even personalized routines embedded in EPROMs. One could also provide variety of interfaces including A/D or D/A devices of a needed accuracy or speed.

Secondly, the proposed scheme could provide opportunities for achieving top performance in a cost effective way. This would be possible by applying the appropriate design of both substrate and performance critical system components to partition the system which would:

1. Use the most expensive technology to fabricate only those components of the system which do need and can take advantage of opportunities provided by modern ULSI;
2. Minimize communication bandwidth bottle necks by using as many as necessary connections nets between system's components;
3. Address the testing problem of traditional MCMs;
4. Address power dissipation problems.

Finally it should be noted that 2.5-D system integration scheme could be very attractive from a "value added" point of view. It could provide opportunities to add value through minimization of time to market (through the ability for prefabrication), through optimization of hardware-software customer oriented co-design and through custom design of small but critical portions of the system. Also this scheme should allow advantage to be taken of the situation created in commodity markets, especially the memory market, where low profit margins will exist as long as there will be a need for large semiconductor houses to compete one with another.

3.3. Smart Substrate MCMs - A Solution to System Yield Problem

Note that the 2.5 D integration strategy may help to solve the system yield problem already mentioned and discussed in the literature in detail. Traditional solutions to this problem assume that acceptable system yield can be achieved by using "Known Good Die". In other words, this approach assumes that for extra cost one can "completely" test IC dice and in this way the probability of the system failure can be kept at an acceptable level. (Discussion of the correctness of a such assumption is beyond the scope of this

paper.) The solution to the MCM system yield problem proposed in this paper is based on the opposite assumption i.e. an assumption that MCM system components are incompletely tested and therefore system integration strategy should accommodate defective dice without affecting system level yield. Such strategy, using concept of 2.5 D integration schema described above, is the main subject of this paper. It is based on the assumption that one can use active substrates to perform testing and assembly in a "smart" way, allowing the detection of defective dice instead of demanding defect free dice. The MCM system which incorporates the above "smart" testing strategy is called in this paper "Smart Substrate System".

In general terms the Smart Substrate System (S^3) MCM is an active substrate MCM designed and fabricated with system/component testing issues in focus. More specifically the smart substrate integration strategy postulated in this paper assumes that active substrate is used - among other things - to perform incremental assembly and testing, conducted in a manner allowing for the system/component level testing after each new component is connected to already operational portion of the assembled system. Such key functionality can be achieved in a number of different ways. One of them is the application of a boundary scan (or BIST) in the active substrate. Another one would be circuitry facilitating direct access of internal system pins through the system level I/Os. In both cases, one would be able to test newly attached dies and in this way:

1. Enable efficient testing of both system components and system-component interfaces.
2. Preclude assembly of incompletely operational system components.
3. Enable rework immediately after detection of a detective component.

The major potential drawback of the Smart Substrate concept is the cost of the substrate itself, especially because its large size makes it susceptible to low manufacturing yield. A key premise of the Smart Substrate concept, however, is that the MCM substrate will have a relatively low density of active components, which will allow relaxed design rules to be used and will lead to acceptable levels of yield. This premise is based on the fact that not the substrate size, but the active area will determine the level of substrate yield loss. Since the substrate performs only routing and support functions for the component dies, the area of the substrate which is actually utilized is expected to be a small fraction of the total substrate area.

Note that the trade off which determines economic viability of smart substrate concept involves two cost components: the cost of the substrate itself and potential yield gains which can be achieved through the testing features implemented in the substrate. A cost modeling technique capturing the above trade-off has been proposed [GaMT94].

Details of the study using this model are outside the scope of this paper. The main conclusion of this study indicates, however, that for many system configurations and performance requirements, MCM Smart Substrate System technology provides an economically-attractive alternative to system design methods being employed today. It was therefore worthwhile to further investigate the technical aspects of the implementation of S^3 MCMs. The remainder of this paper summarizes a design case study involving a small Smart Substrate System.

4. MCM SMART SUBSTRATE SYSTEM CASE STUDY

A prototype MCM Smart Substrate System has been designed and fabricated to demonstrate the technical feasibility of the MCM S^3 methodology and study the basic circuit solutions which may be needed in complex MCM Smart Substrate Systems. This section presents summary of the obtained results.

4.1. System Description

The implemented prototype is a functional equivalent of National Semiconductor's hybrid microcontroller emulator COP881CMH. It is composed of two commercial dies (National Semiconductor COP820 microcontroller and an Atmel 64k EEPROM) which were bonded to a custom-designed CMOS substrate carrier. The active substrate contains both the interconnect and glue logic necessary for appropriate communication between the commercial dies and "Smart" testing logic. The testing logic can be used to incrementally test the system components (including the substrate) during system assembly.

Figure 3 shows a drawing of the top view of the prototype system assembly. The whole system is packaged in a 132-pin ceramic pin grid array. The Smart Substrate die is wire bonded into this package, and the two commercial dies are glued and wire bonded onto the already-packaged substrate die. (The decision to use wire bond assembly for the prototype system was driven solely by technology availability.) Figure 4 shows a photomicrograph of the manufactured, assembled system.

The basic microcontroller emulator system is shown in Figure 5. Figure 6 shows the details of the glue logic circuitry. The glue logic was designed to support three modes of operation: direct memory write, direct memory read, and COP-memory communication during normal system operation.

4.2. Testing Strategy

In addition to the basic circuitry shown in Figure 5, the prototype system also contains Smart testing logic. It was designed to provide:

1. Separate direct access to each die in the system;
2. Boundary-scan testability of both component dies and the substrate interconnect and glue logic;
3. Boundary-scan testability of the enhanced-memory controller system as a single circuit (for potentially facilitating subsequent board test);
4. Selective control of which sections of the system are powered during testing.

The above features enable individual testing of each component within a fully (or partially) assembled MCM S^3.

Figure 7 shows the full circuit block diagram of the prototype system, including all built-in "Smart" testing features. The chip can be operated in any of the supported testing modes or in "normal mode", in which no testing features are enabled.

The most basic of the testing modes implemented is direct access. This mode is controlled by a single "direct access" control signal which is accessible from the MCM package boundary. In this mode, all pins of the COP chip and all pins of the memory chip are accessible through package pins. (In a larger MCM S^3 this option would have to be modified since the total number of MCM package pins may not be sufficient to assure direct access for all system components at once.)

The boundary-scan testing feature is realized by three separate boundary scan chains, each dedicated to one component of the system. (In a larger system design access to these chains would be coordinated through a central test controller.) The boundary scan cells implemented in this prototype support the JTAG-compatible test functions of INTEST (for isolated testing of dies in the system), EXTEST (for testing the communication logic implemented in the substrate die), and SAMPLE (for taking a snapshot of the system's operation as it runs at speed).

Finally, the Smart logic in the prototype system allows for selective connection of power to the chips in the system. This feature facilitates incremental test during system assembly, and also allows for selective I_{ddq} testing of components in the system.

4.3. Testing Circuitry

The above described testing strategy have been implemented using following circuit solutions.

4.3.1. Boundary scan cells

There are three basic variations of the boundary scan cell which are used in our design. The first is placed in uni-directional signal paths which always run from the substrate to a die (or to a package pad). The second is placed in uni-directional paths which run from the in-system chips (or package pads) to the substrate. The third is placed in bi-directional data paths. Each of them has the following features.

Uni-directional boundary scan cells. Figure 8 shows the details of the die-to-substrate and substrate-to-die boundary scan cell. Note that in both cases, the "normal" circuit connection through the cell conducts only when the boundary scan chain is neither in INTEST mode nor in EXTEST mode. Note also that in each cell, the scannable latch drives onto the system signal line only as appropriate for each testing mode. Figure 9 comprehensively shows the connections which are implemented in both uni-directional boundary scan cells for each mode of operation of the test circuitry. In the drawings in this Figure, the emboldened lines represent the circuit paths which are conducting, for each testing mode.

The bi-directional boundary scan cell. In our design, as in Smart MCM systems in general, the bi-directional boundary scan cells pose a particular problem. The problem is that there is often no control signal which clearly states whether a bi-directional pin on a die is driving or sensing at any particular stage of the die's operation. For example, in this prototype system, the COP chip G and L (see Fig. 5) ports may be configured pin-by-pin to be either output or input ports on the chip. The directionality of the pins in these ports is determined by a value stored in a memory-mapped status register internal to the COP processor. There is, therefore, no simple way to determine whether the G and L port pins are input pins or output pins at any particular stage of the system's operation.

In general, the bi-directional boundary scan cells must be designed assuming that signals can be driven in either direction on the signal buses. That is, the boundary scan cell cannot contain any directional circuitry in the data path (such as tri-state buffers), since in general it is impossible to generate a control signal for the enable input of the tri-state circuitry. Note that this problem is not addressed by the IEEE JTAG test standard, since the boundary scan cells in this standard are assumed always to be implemented internally to the chips. Hence, there will always be a control signal which indicates the directionality of any

given pin on the periphery of the chip.

Therefore, the Smart bi-directional boundary scan cell may introduce only a transmission gate into the datapath. The transmission gate conducts for normal circuit operation and does not conduct during INTEST and EXTEST testing modes. The circuit schematic which implements the bi-directional boundary scan cell is shown in Figure 10. The scannable latch used in the bi-directional boundary scan cell is the same as that used in the uni-directional cells.

4.3.2 Selective power connection

Finally, our prototype system allows for selective connection of power to the chips in the system. This feature facilitates incremental test during system assembly, since any subset of (not-yet-populated) chip sites in a Smart system can be left un-powered during testing.

The prototype system was designed for and manufactured in a p-well CMOS technology. Therefore, Vdd is global to the system substrate. The selective power capability was implemented by partitioning the GND network in the prototype. Four partitions were chosen: one GND net for each of the COP chip, the memory chip, the glue logic, and the substrate die pad drivers. In all cases, the power connections for boundary scan cells (and direct access transmission gates) are associated with the nearest substrate pad driver. In Figure 11, the light gray shading illustrates which components of version two of the system are powered by each separate GND pin.

4.4. Testing Strategy

The incremental tests for Smart Substrate System prototype (and in general to any MCM S^3) is envisioned as being performed in three major steps:

Step 1. Testing of unpopulated substrate.

In this step (performed as a probe test on the wafer with the substrate dies) one should determine fault free operation of the substrate itself. In the case of the prototype system described in this paper such goal is accomplished by using:

- boundary scan testing of the in-substrate glue logic in EXTEST mode
- boundary scan chain function as shift register

With the extra testing pins one also would be able to perform testing of

direct access mode of testing by probing continuity from package pins to chip pins.

Step 2. Testing of partially populated substrate

In this step, performed on the substrate die assembled in the MCM package, subsequently attached chips could be tested for :

a. I/O continuity;

b. Functionality;

c. Communication with previously attached system components.

For this purpose one could use boundary scan or direct access circuitry. In the case of the prototype system discussed in this paper such testing could be performed on the substrate with either memory or COP chip attached. For memory testing one would perform:

- all tests described in Step 1 and
- memory test through the glue logic;
- memory test through direct-access for all functionality;
- boundary scan access to memory in INTEST mode - writing and reading.

For COP testing one would perform:

- all tests described in Step 1 and
- test of interface with glue logic through boundary scan access to COP chip in INTEST mode;
- direct-access test for COP functionality;
- system partial test by clocking COP chip and using boundary scan logic to SAMPLE signal values in the system.

Step 3. Testing of fully populated MCM S^3

In this step final system tests test would be performed. Essentially, it could be executed as a standard system test supported by the boundary scan. In addition direct access testing could be conducted as well. This option could be used for system diagnosis purposes. In the case of microcontroller discussed in this paper one could perform:

- direct access test of each chip in system individually;
- boundary scan test of each chip in assembled system (INTEST mode);
- boundary scan test of glue logic in assembled system (EXTEST mode)
- at speed system test using boundary scan and SAMPLE operation running the

system at full speed.

Notice that by executing test in the above manner, i.e. by combining test and assembly operations, one can detect faulty components immediately after assembly. Consequently, diagnosis and rework are simple and much more effective maximizing this way system level yield.

4.5. Future Possible Testing Enhancements

Application of the active substrate in the MCM systems provides a large spectrum of testing opportunity not implemented in the MCM S^3 described in this paper. Some of them should be mentioned, however, to highlight positive characteristics of the Smart Substrate concept.

First, and the most obvious enhancement of the testing methodology discussed in this section would be application of memory and micro-processor BIST built directly into the substrate of an MCM S^3. Second would be enhanced control over chaining of the different subsets of boundary scan cells. This control should be encapsulated in a single test access port controller. Additional functionality could also be added to conform to the standards implemented in the TI SCOPE Test Bus Controllers [Te91] and Probe chip [Ba92] architecture. Finally, sophisticated application of JTAG-compatible boundary scan within an MCM S^3, including compatibility with new JTAG mixed-signal testability standards [IEEE 1149.5] should also be considered

The other area of opportunity for MCM S^3 application would be in defect- and fault-tolerant systems. In such systems on-the-fly error sensing and context saving using BIC sensors for concurrent system monitoring could be used to detect and predict failure of system due to latch-up, transient radiation faults, etc.

Notice, finally that with MCM S^3 all of the above testing options can be available with out redesigning system's components. This indicated that MCM S^3 enables "virtual" BIST technique which could be applied with "non-BISTed" components.

5. CONCLUSIONS

To motivate the study presented in this paper it was determined that the keys to the economical manufacture of MCMs will be: (1) the ability to test bare dies at speed for the

system environment into which they will be assembled, (2) the ability to make use of existing dies (without modification) in the design an MCM system, (3) the ability to inexpensively re-work the placement of system-killing bad die(s) in an MCM during system assembly, and (4) the ability to use dies of a variety of fabrication technologies in the same system. The prototype MCM Smart Substrate system described in this paper represents the results of the first implementation study of a design methodology which has the capability of addressing all of these issues in a cost-effective manner.

Through this study, the feasibility of MCM Smart Substrate Systems has been demonstrated. Furthermore, a number of circuit design issues, which facilitate independent testing of a partially-assembled system, have been solved as a direct result of having undertaken this study. Finally, it should be noted that initial cost analyses conducted during this study have indicated that MCM S^3 design can be an economically-attractive alternative to traditional MCM, PCB or WSI system implementation technologies which are currently being utilized.

Acknowledgments

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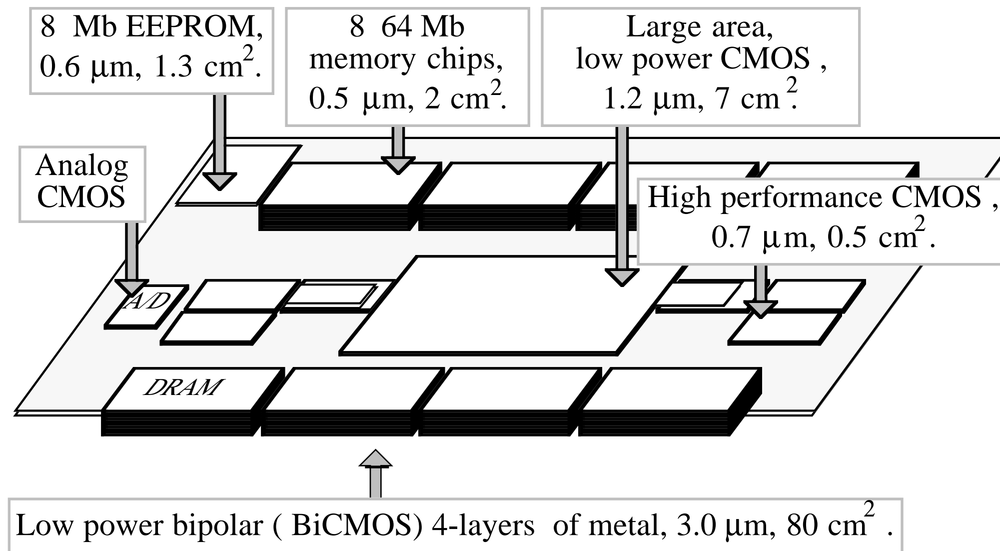


Figure 1. Example of a system using active substrate.

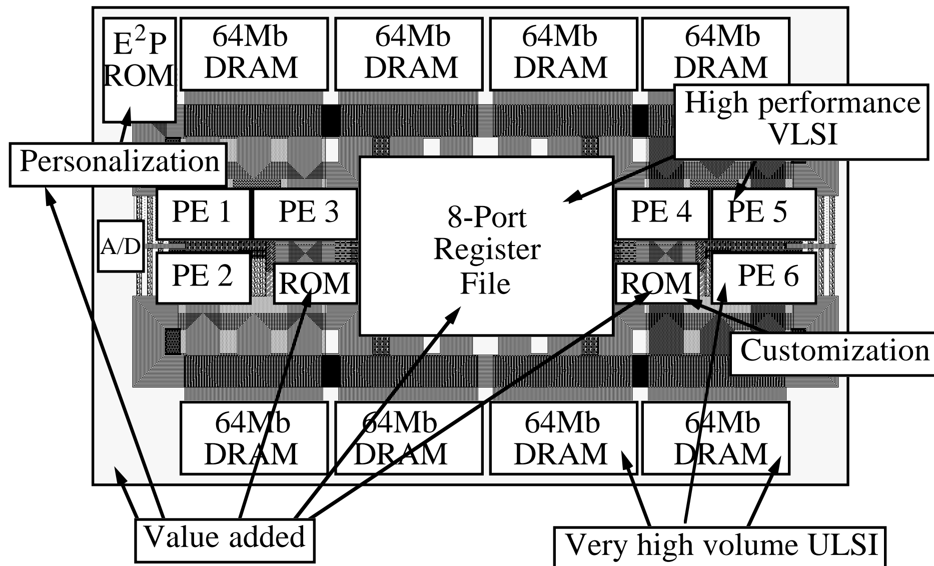


Figure 2. Essential attributes of a system implemented with 2.5-D integration scheme.

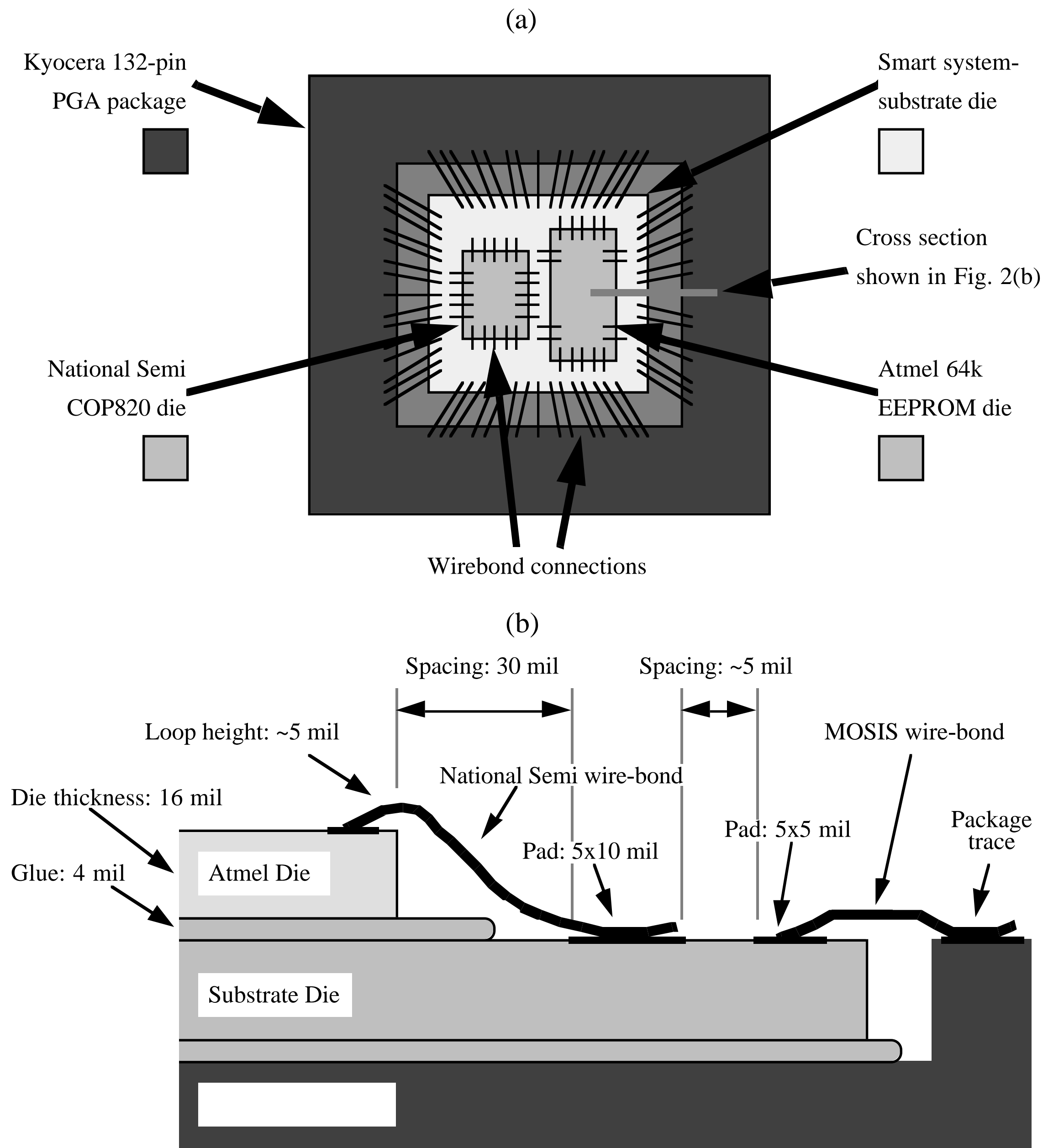


Figure 3 – Prototype system packaging technology. (a) PGA package top view and (b) wire-bonding cross section with dimensions (not drawn to scale).

Figure 4 – Photograph of the Smart Substarte prototype.

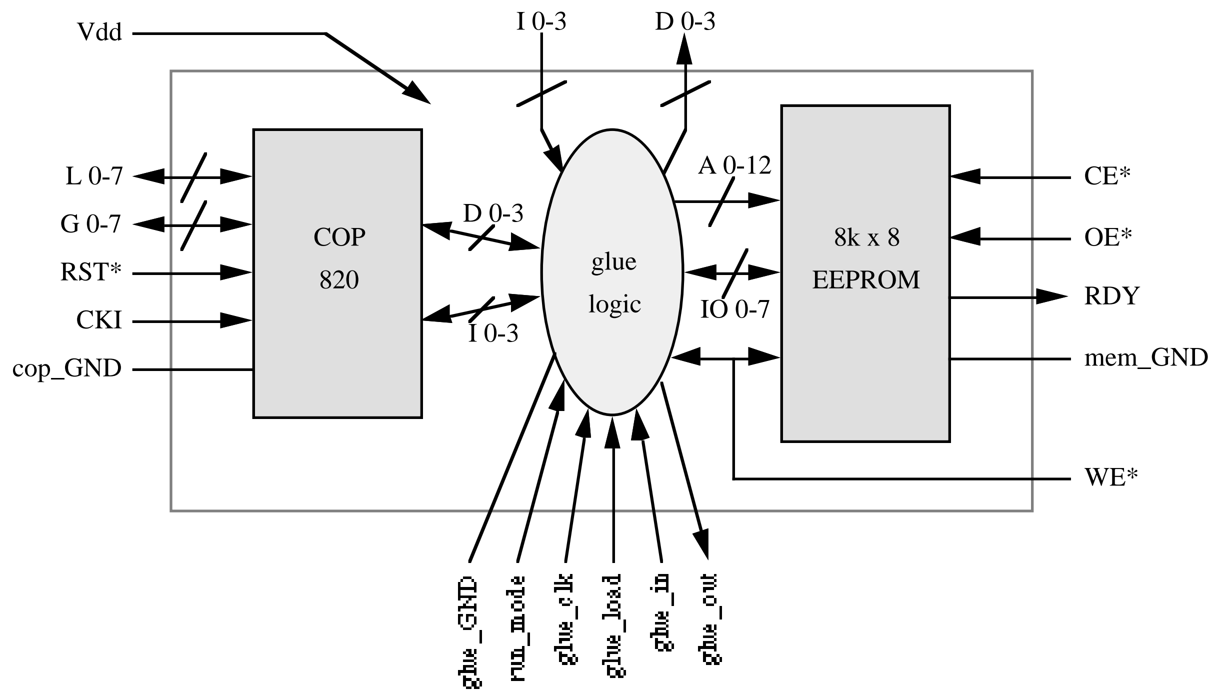


Figure 5 – Prototype system block diagram

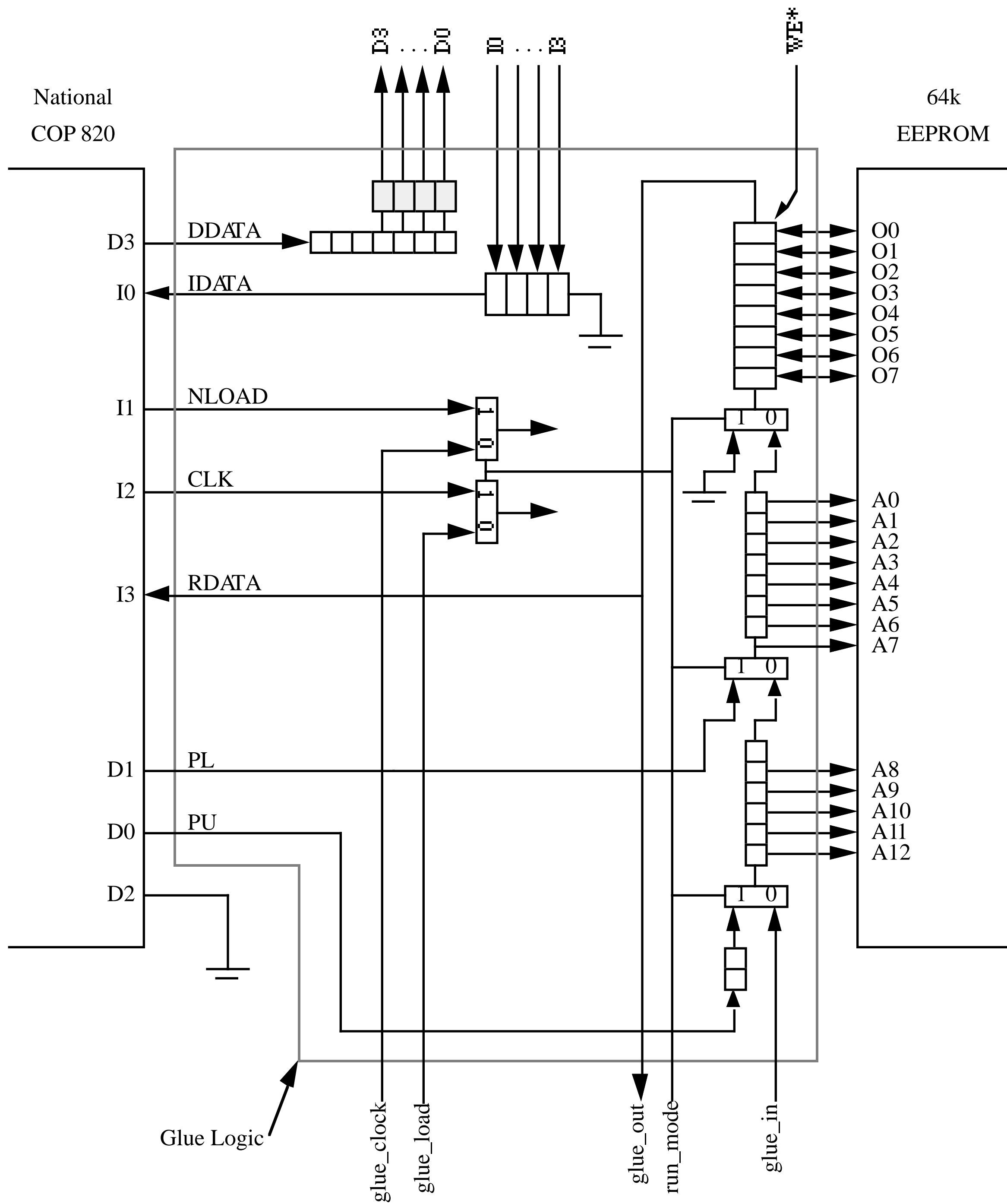


Figure 6. Glue logic circuitry in the prototype system.

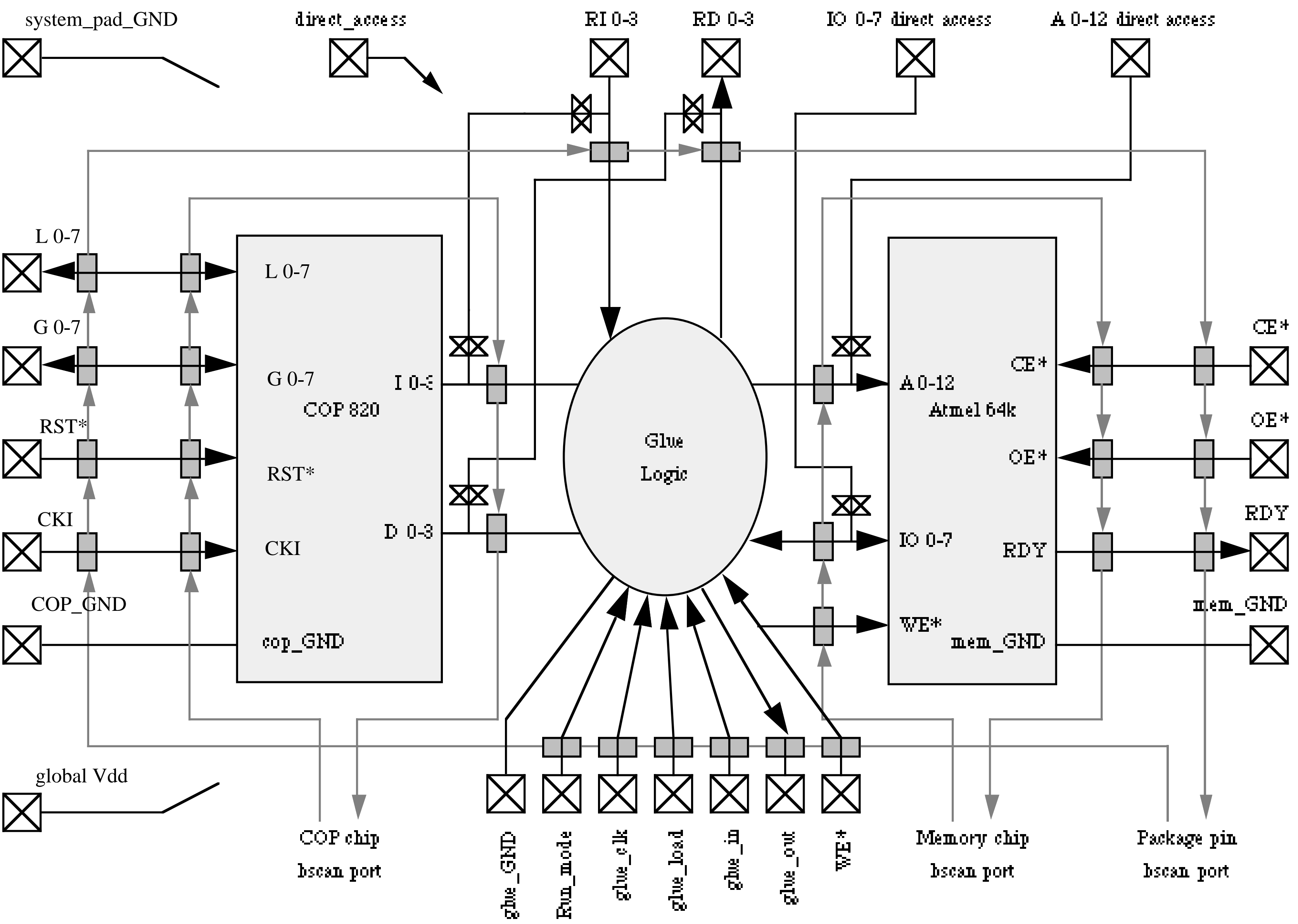
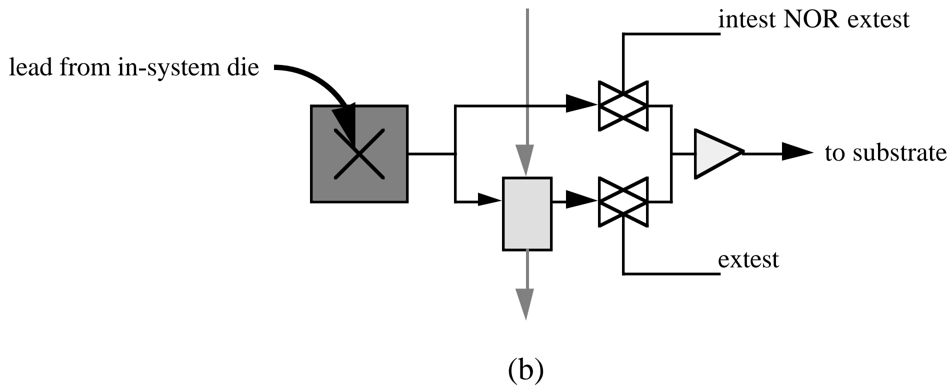
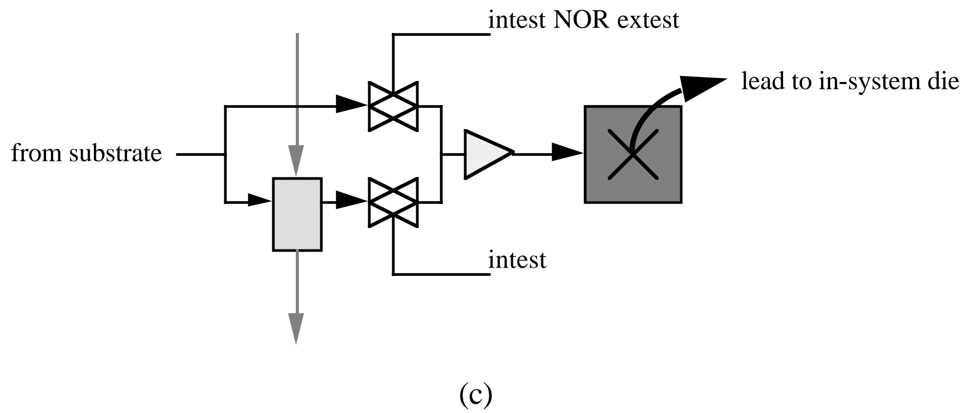


Figure 7 - Block diagram of Smart Substrate prototype system.

(a)



(b)



(c)

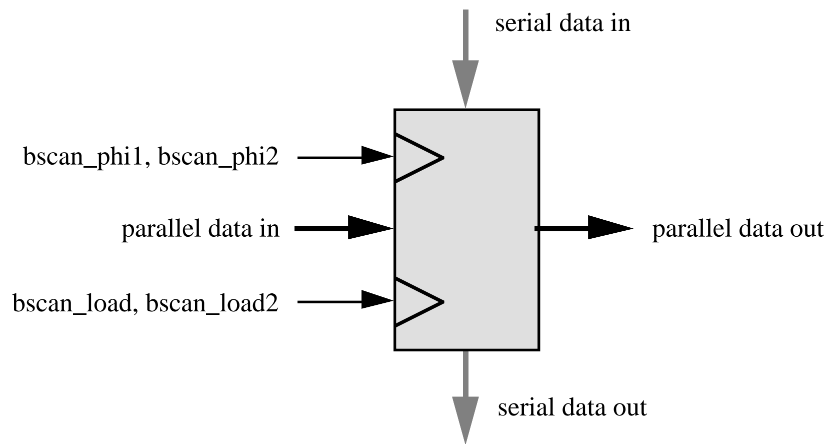


Figure 8 – Implementation details for uni-directional boundary scan cells. (a) boundary scan cell: die-to-substrate connection. (b) boundary scan cell: substrate-to-die connection. (c) scannable latch subcell.

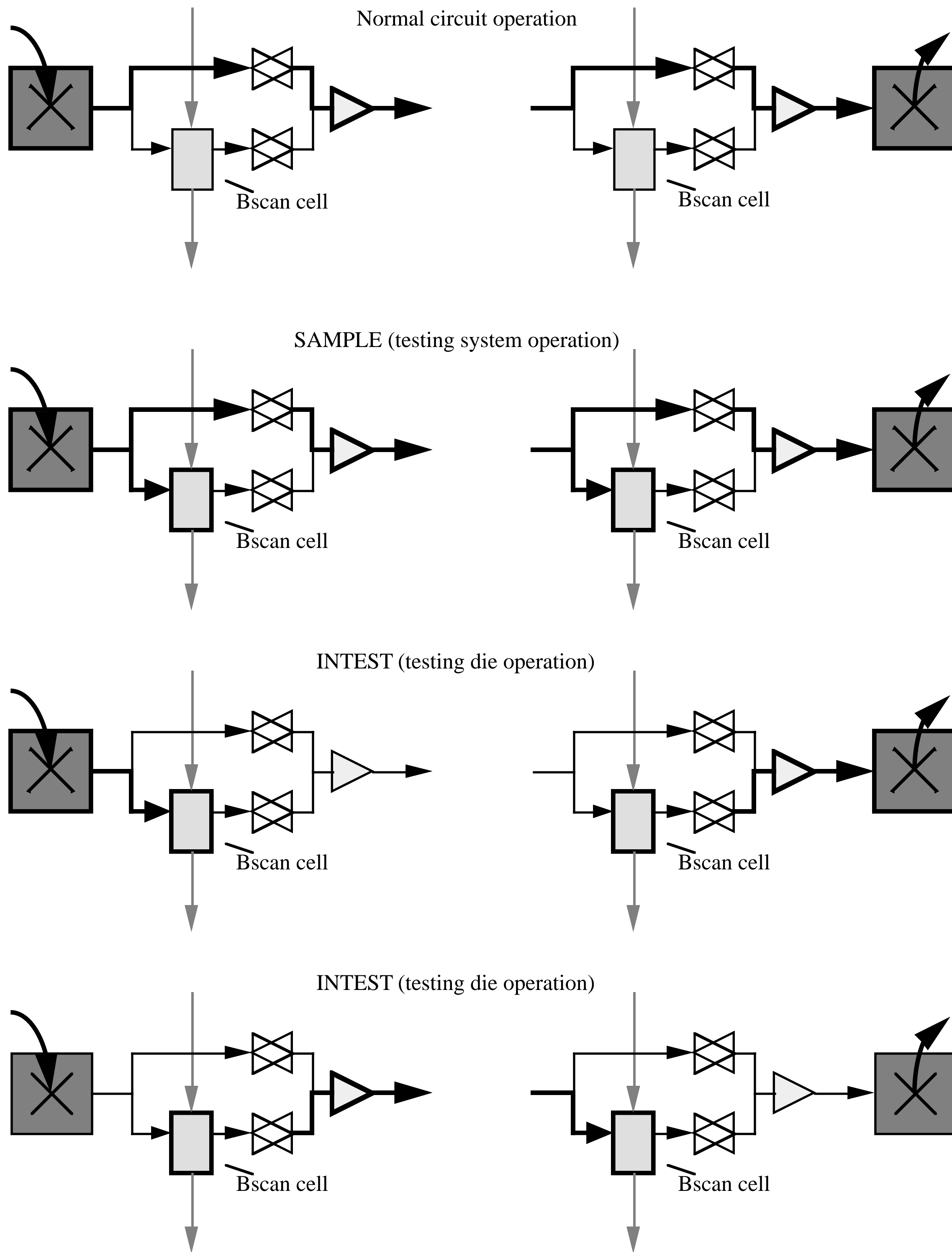
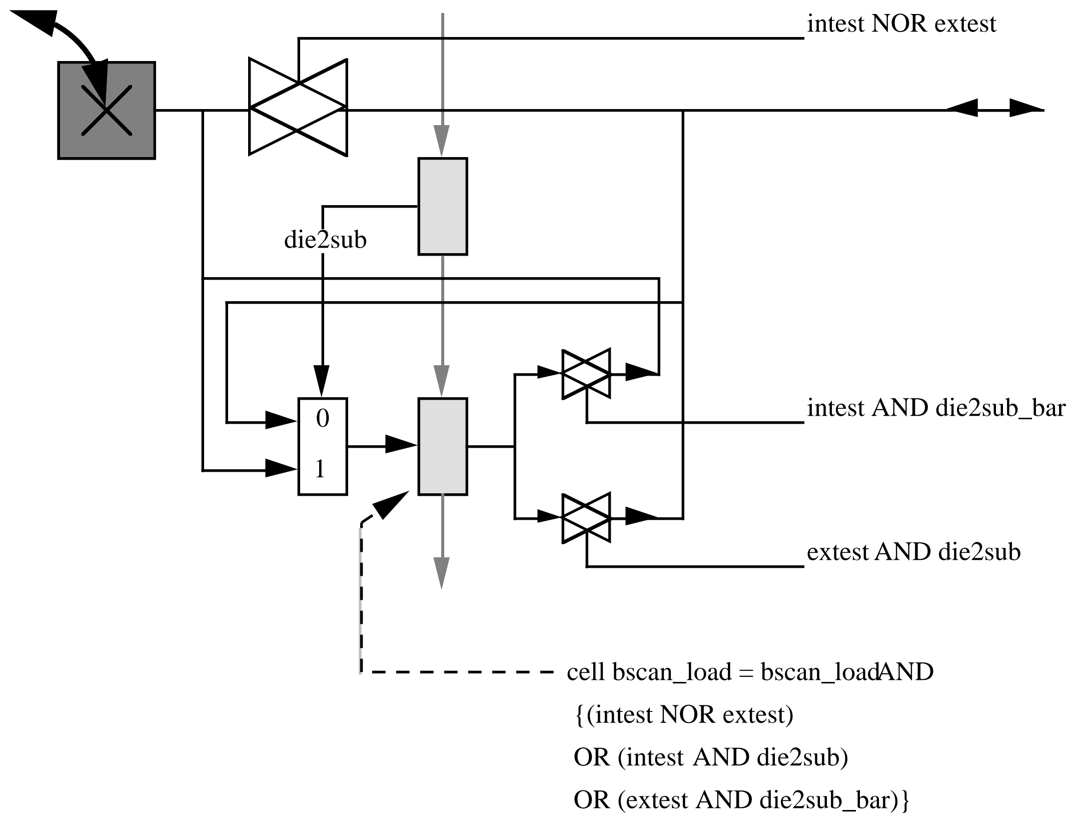
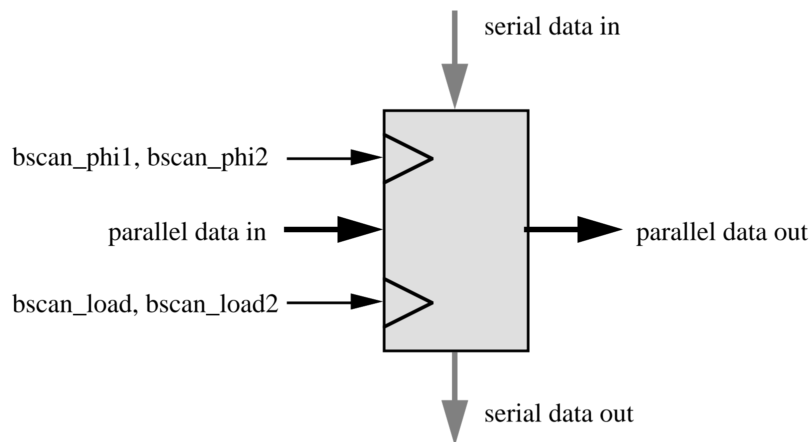


Figure 9 – Testing modes of uni-directional boundary scan cells.



(a) The bi-directional boundary scan call



(b) Scannable latch subcell

Figure 10 – Circuit schematic for the bi-directional boundary scan cell. (a) schematic and (b) scannable lach subcell.

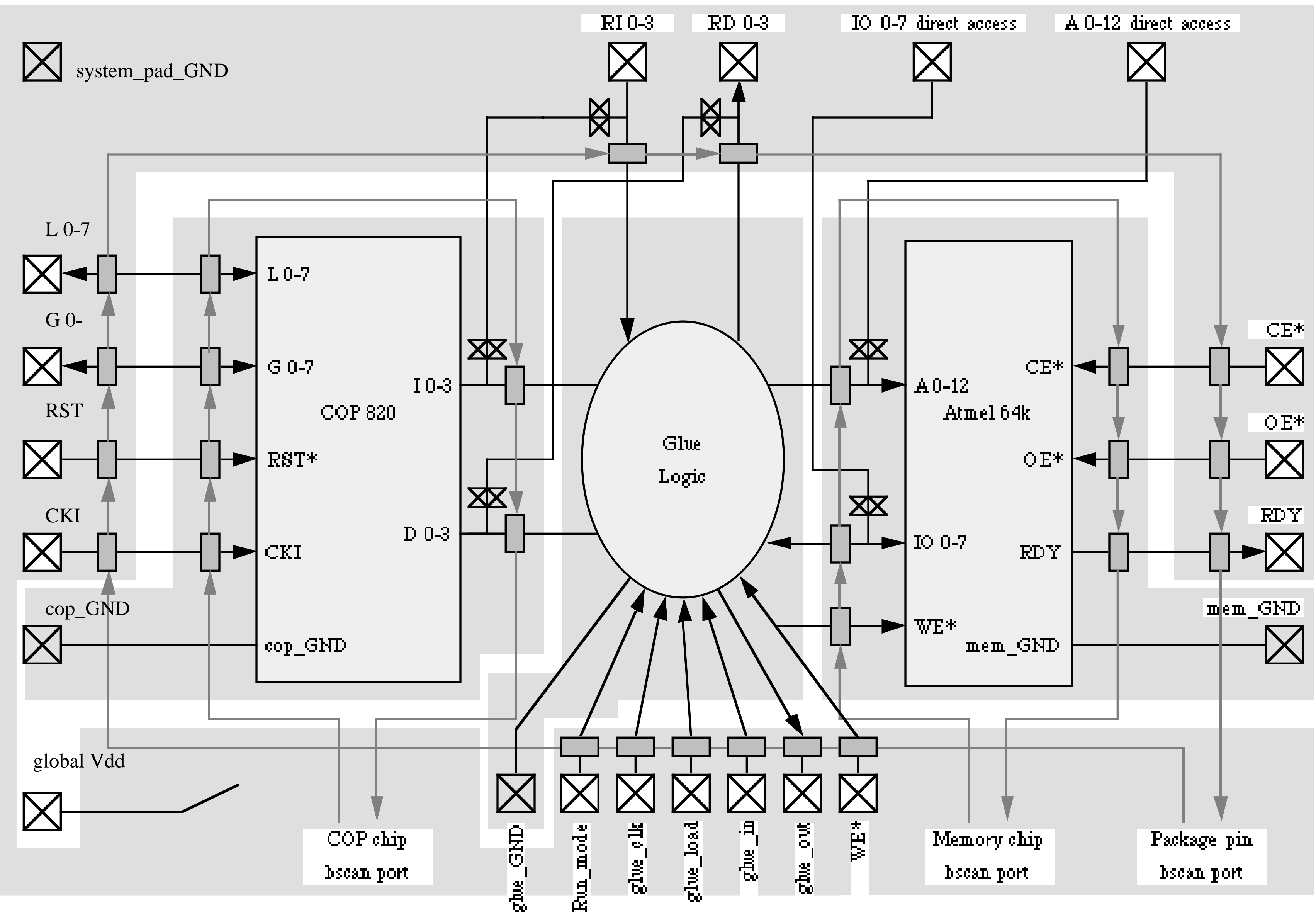


Figure 11 – Ground connections in the Smart prototype