

Coding and Signal Processing for Holographic Data Storage

Prof. Vijayakumar Bhagavatula
Data Storage Systems Center (DSSC)
Carnegie Mellon University, Pittsburgh, PA, USA

Holographic data storage (HDS) appears to be on the verge of becoming a viable data storage technology, albeit with niche markets in the early stages. HDS differs significantly from both magnetic and conventional optical data storage in many ways including: volumetric nature of the storage, page-oriented writing and reading, the use of input devices (spatial light modulators or SLMs) and output devices (cameras) mainly designed for other applications (SLMs for displays and cameras for home use) and non-stationary channel response due to the fact that optics is much better closer to the optical axis than away from it. Thus HDS offers its own advantages (higher volumetric densities, faster data rates, rapid access and archivability) and challenges (low SNR, 2-D inter-symbol interference, SLM/camera mis-alignment, optical noise, channel response non-stationarity, etc.). In what follows, we will summarize our prior research contributions in this area and briefly discuss some relevant research topics we plan to pursue.

We have been a part of both the DARPA-funded 5-year Holographic Data Storage System (HDSS) project as well as the more recent NIST-funded 2-year ATP program on holographic data storage led by InPhase Technologies. In both these efforts, our role has been in developing and evaluating the coding and signal processing methods for HDS. One post-doc (Dr. Zongwang Li), three Ph.D. students (Venkatesh Vadde, Mehmet Keskinöz and Lakshmi Ramamoorthy) and two Master's students (Magdalena Wong and Sheida Nabavi), working with Prof. Kumar, have made several contributions to HDS including:

- Developed a **HDS channel model** [1] that takes into account the optical noise, the electronic noise (from the camera), the 2-D inter-symbol interference and the nonlinear intensity detection due to the camera.
- Developed a **channel identification method** [1] that estimates the channel point spread function (PSF) from sample input pages and corresponding output pages obtained from real HDS systems.
- Developed a **MATLAB-based HDS simulator** [2] that includes impairments such as: finite SLM contrast ratio, SLM non-full fill factors, non-flat illumination, non-uniformity among SLM pixels, apertures in the frequency plane, camera pixel non-uniformity, camera pixel non-full fill factors, quantization in camera output, optical noise, electronic noise and non-stationarity.
- Developed **2-D linear** (e.g., zero-forcing, minimum mean squared error and decision feedback) **equalization** schemes [3] and **evaluated** them using real data pages as well as synthesized pages.
- Developed and evaluated **2-D nonlinear equalization** [4] methods that take into account the nonlinear nature of the HDS channel.
- **Evaluated existing 2-D data detection methods** (e.g., Viterbi in one direction and decision feedback in the other direction) and introduced a new detection method (called **iterative magnitude squared decision feedback**) [5] that takes into account both the 2-D nature of the HDS channel and the intensity detection nonlinearity due to the output camera.
- Developed a new modulation coding method called **parity coding** [6] that may offer a more efficient method for dealing with illumination changes over a data page (a problem usually addressed using sparse codes).
- Developed new **hardware-friendly quasi-cyclic low density parity check (QC-LDPC) codes** [7] of long length (32 Kb) that exhibit significant performance gain (4 to 6 dB) over uncoded HDS channels.
- Developed a **C-language software module to design QC-LDPC codes** for specified code rates and codeword lengths.
- **Developed and implemented an FPGA architecture** for the encoder and the decoder of QC-LDPC codes

Based on our experience with real HDS data, it does not appear that at current storage densities, inter-pixel interference is a major problem. Thus equalization techniques may not benefit much. On the other hand, SNRs appear to be pretty low and thus powerful error correction schemes (to provide SNR gains of about 6 dB) are needed. It is important to model realistic noise and impairments in evaluating the SNR gains. Also, because of the non-stationary nature of channel responses, interleaving may offer benefits. Another important problem is that the input page must satisfy constraints such as sparseness or balance. The conventional sparse codes or balanced codes use hard decoding (where the output of the decoder is either a 1 or 0) whereas LDPC decoders need as their input soft information (e.g., probability that a particular bit is a 1 or 0). Finally, since SLM and camera pixel pitches will be different and since it is nearly impossible to maintain the desired magnification over the entire field of view, there will be mis-alignment between SLM pixels and camera pixels. To provide advanced solutions to these problems, we are pursuing the following HDS research tasks.

1. **Design of QC-LDPC codes** of various rates and various codeword lengths suitable for HDS page blocks,
2. **Evaluation of the various QC-LDPC codes using the FPGA platform** in order to quantify the SNR gains,
3. **FPGA-based synthesis of HDS readback pages** with realistic noises and impairments for rapid evaluation of codes,
4. **Design and evaluation of interleaving strategies** optimized for the non-stationarity of HDS channels,
5. Development and evaluation of **sparse coding schemes that are compatible with LDPC codes** employing iterative soft decoding,
6. Development and evaluation of **reduced-complexity re-sampling schemes to cope with SLM/camera mis-alignment**.

References

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