18-447 Lecture 10: Branch Prediction

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• Your goal today
  – understand how to guess your way through control flow and why it works so well

• Notices
  – Lab 2, status check this week, due next week
  – HW2, due Wed
  – Midterm, next Monday, cover up to Lec 9

• Readings
  – P&H Ch 4
Branch Prediction 101: PC+4

In general as long as
1. prediction is always checked
2. correct target is fetched after a misprediction
3. wrong path instructions removed

**ANY** predictor will work, including RNG, PC-4

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**Diagram:**
- $\text{Inst}_h$ is a taken branch
- Control flow "restitched"
- $\text{IF}_{\text{PC}}$, $\text{IF}_{\text{PC}+4}$, $\text{IF}_{\text{PC}+8}$
- $t_0$, $t_1$, $t_2$, $t_3$, $t_4$, $t_5$
Prediction and Resolution (in-order pipeline)

- “Trust, but verify”
- When wrong, (1) clean up mistake and (2) update predictor to improve next guess

```
PC → I-mem → fetched PC → Inst → actual target
```

```
nextPC → "ANY" branch predictor

• pred. target
• pred. taken?
• mispredict?
```

```
rewind
```

```
update
```

```
compute actual outcome
```

```
actual target
```

```
kill kill kill
```

```
mispredict?
```

```
??
```

```
update
```

```
3
```

```
3'
```

```
3''
```

```
1
```

```
2
```

```
3
```

```
3'
```

```
3''
```

```
??
```

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Tagged BTB (from last lecture)

\[
\text{IPC} = \frac{1}{1 + (0.20 \times 0.3) \times 2} = 0.89
\]

if not taken
Branch Prediction Recap

- Given current PC, choose most likely next PC
- The easy part: target
  - same PC always same instruction
  - nextPC always PC+4 for non-control-flow inst
  - target of PC-offset control-flow always same
    BTB from last lecture works very well
- The not so easy part: taken?
  - branch decision is dynamically data dependent
  - so far, either 1. always-predict-not-taken (PC+4) or
    2. always-predict-taken (BTB)
Branch Direction Prediction

- Already 100% correct on non-control-flow inst
- Improve on always-predict-taken (70% correct)?
  - ~90% correct on backward branch (dynamic)
  - only ~50% correct on forward branch (dynamic)

  What pattern to leverage on forward branches?

- A given static branch instruction is likely to be biased in one direction (either taken or not taken)
  - 80~90% correct (forward+backward) if guessed to repeat the outcome last time
  - \[ \text{IPC} = \frac{1}{1 + (0.20 \times 0.15) \times 2} = 0.94 \]
    \[\text{if not repeat}\]
“Adaptive” History-Based Prediction

Branch History Table entry is updated with actual outcome after branch is executed.
Branch History State Machine

Predict same as last outcome
2-Bit Saturation Counter

How is this better?
2-Bit “Hysterosis” Counter

Change prediction after 2 consecutive mistakes
Per-Branch Counter-Based BP

- 2-bit counter can get >90% correct
  - IPC = \( \frac{1}{[1 + (0.20 \times 0.10) \times 2]} = 0.96 \)
  - any "reasonable" 2-bit counter works
  - adding more bits to counter does not help much

- Major branch behaviors exploited
  - almost always repeat the same (>80%)
    - 1-bit and 2-bit counters equally effective
  - occasionally do the opposite once (5~10%)
    - 2 misprediction with a 1-bit counter
    - 1 misprediction with a 2-bit counter

- Need more elaborate predictors for other behaviors

\textit{Is it worth the cost? Will it slow down the clock?}
The cost of misprediction

- Misprediction penalty increases with
  - number of pipeline stages
  - width of superscalarity
  - number of nested predictions and rewind cost

[“The microarchitecture of the Pentium 4 processor,” Intel Technology Journal, 2001.]
Multiple shots at better predictions

- more time & info in later stages
- early "correction" based on better guesses

- Prediction Logic (4 instructions)
- Target
- Seq Addr

- PC
- +

[PowerPC 604]
Two-level Prediction [Yeh & Patt]

- **tag**
- **BTB idx**

- **m-bit “local” branch history**
  - e.g., if $m=6$
  - 000000
  - 111111
  - 101010
  - 110110
  - 101101
  - 011011

- **isBranch?**
- **taken?**

what a branch did last $m$ times

what happened for a pattern?
Path History

• Branch outcome may be correlated to other branches

• Equntott, SPEC92

```c
if (aa==2) ;; B1
    aa=0;
if (bb==2) ;; B2
    bb=0;
if (aa!=bb) ;; B3
    { .... }
```

• If B1 is not taken (i.e. aa==0@B3) and B2 is not taken (i.e. bb=0@B3) then B3 is certainly taken

How to capture this information?
Global Branch History Shift Register tracks the outcomes of the last M branch instructions
Return Address Stack

• A register-indirect jump can have different target
  – same target only if fxn called repeatedly from same call-site
  – but, function call and return behavior easily tracked by a last-in-first-out queue

• Return Address Stack
  – return address is pushed when a link instruction (e.g., JAL) is executed
  – when encountering PC of a return instruction (e.g., JALR) predict nPC from top of stack and pop

What happens when the stack overflows?
How do you know when to follow RAS vs BTB?
Alpha 21264 Tournament Predictor

- Make separate predictions using local history (per branch) and global history (correlating all branches) to capture different branch behaviors
- A meta-predictor decides which predictor to believe

Better than 97% correct
Superscalar Complications

- “Superscalar” processors need to fetch multiple instructions per cycle
- Consider 2-way superscalar fetch scenario
  
  **(case 1)** both instructions are not taken control-flow
  - \( nPC = PC + 8 \)

  **(case 2)** one inst is a *taken* control-flow inst
  - \( nPC = \) predicted target addr

  *note: both instructions could be control-flow; target is for younger of predicted taken*
  
  - if 1\textsuperscript{st} instruction is predicted taken, nullify 2\textsuperscript{nd} instruction fetched
2-way Branch Predictor Sketch

- Tag Table
- Branch History Table (BHT)
- Branch Target Buffer (BTB)

- Cache block offset
- Last inst in cache block?
- Hit
- First?
- Taken?
- PredPC

- PC+4
- PC+8
Intel P4 Trace Cache

- A 12K-uop trace cache in place of L1 I-cache
- 6-uop per trace line, can include branches
- Trace cache returns 3-uop per cycle
- IA-32 decoder can be simpler and slower

Diagram:

- Front End BTB (4K Entries)
- ITLB & Prefetcher
- IA32 Decoder
- Trace Cache BTB (512 Entries)
- Trace Cache (12K uop’s)
- L2 Interface
Ways SW can Help

• Associate static branch “hints” with opcodes
  – taken vs. not-taken
  – whether to allocate entry in dynamic BP hardware
• Give SW and HW joint control of BP hardware
  – Intel Itanium BRP (branch prediction) instruction
    issued ahead of branch to preset BTB state
• TAR (Target Address Register, Itanium)
  – a small, fully-associative BTB
  – controlled entirely by BRP instructions
  – a hit in TAR overrides all other predictors

Eliminate “urgency” created by not computing branch condition and target until last inst in basic block
Predicated Execution

- Intel Itanium example
  - predicate register file (64 by 1-bit)
  - each instruction has a predicate reg argument
  - instruction is NOP if predicate is false at runtime
- Converting control flow into dataflow

Make sense if processors have lots of spare resources and BP is hard
Next time: Interrupt Control Transfer

- **Basic Part:** an “unplanned” fxn call to a “third-party” routine; and later return control back to point of interruption

- **Tricky Part:** interrupted thread cannot anticipate/prepare for this control transfer
  - must be **100% transparent**
  - not enough to impose all callee-save convention

- **Puzzling Part:** why is there a hidden routine running invisibly?