Heterostructure Si$_{1-x-y}$Ge$_x$C$_y$-channel p-MOSFETs compatible with CMOS processing

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ABSTRACT

We report the fabrication of heterostructure p-MOSFETs with low-carbon Si$_{1-x-y}$Ge$_x$C$_y$ channels. The use of low carbon fraction ($y = 0.002$) does not significantly affect the strain of the channel layer or the valence band offset. Small carbon fractions do improve the thermal stability of the channel region and make it possible to use conventional thermal oxidation and ion implant annealing without layer relaxation. A peak hole mobility of 200 cm$^2$/Vsec was measured in a device with a 30 nm channel and a germanium fraction ramped from 10% to 40%.

Introduction

Several recent studies have addressed the fabrication of heterostructure p-MOSFETs with strained germanium-silicon channels. Changes in the valence band structure in compressively strained germanium-silicon alloys lead to an increased hole mobility in these structures, and in addition the scattering from charges at the semiconductor-insulator interface is reduced. These factors lead to an enhancement in mobility of 30-50% over the field effect hole mobility observed in conventional devices. Unfortunately there are difficult tradeoffs in device design as thick layers with high germanium fraction are desirable in order to increase the channel charge capacity. Such layers may relax during subsequent thermal processing and consequently may be difficult to integrate into conventional CMOS processing.

In this letter we will show that germanium-silicon-carbon channels are more compatible with high-temperature processes such as thermal oxidation and ion implant annealing. In contrast to a recent report, we focus here on low-carbon epitaxial layers ($y = 0.002$). Layers with such low carbon concentrations are more readily grown with full substitutionality and may be less likely to form silicon carbide precipitates during subsequent processing. Carbon concentrations at this level do not significantly alter the strain or band structure of the channel, thus the predominant effect of carbon is to improve the thermal stability of the channel.

Growth and Stability of Si$_{1-x-y}$Ge$_x$C$_y$ channels

Si$_{1-x-y}$Ge$_x$C$_y$ layers were grown by multiwafer UHV/CVD at 550 °C using silane,
germane, and methylsilane (with the last two diluted in hydrogen) as the reactants. As previously reported, the incorporated carbon is fully substitutional up to 0.2% for both Si$_{0.89-y}$Ge$_{0.11+y}$ and Si$_{1-y}$C$_y$ layers. Annealing studies of epitaxial layers which exceeded the equilibrium critical thickness$^7$ showed distinctly different relaxation behavior for layers of similar strain and thickness with and without 0.2% carbon. X-ray diffraction showed significant relaxation at 650 °C for Si$_{0.91}$Ge$_{0.09}$ layers, which was evidenced by broadening of the main layer peak and a decrease in the lattice constant in the direction of growth. In contrast, the Si$_{0.888}$Ge$_{0.11}$C$_{0.002}$ layers were unaffected by anneals up to 900 °C. At higher annealing temperatures the lattice constant in the direction of growth increased, indicating a reduced substitutional carbon concentration. The improved thermal stability of Si$_{1-x-y}$Ge$_x$C$_y$ layers makes it possible to use thermal oxidation and ion implantation annealing and thus makes it possible to incorporate heterostructure MOSFETs in a conventional CMOS process.

We first confirmed the stability of Si$_{1-x-y}$Ge$_x$C$_y$ layers by fabricating heterostructure MOS capacitors. The structures were fabricated on an n-type (100) substrate and consisted of a 5 nm Si$_{0.998}$C$_{0.002}$ layer doped with boron to $1.7 \times 10^{17}$ cm$^{-3}$, a 5 nm Si$_{0.998}$C$_{0.002}$ spacer layer, a Si$_{1-x-y}$Ge$_x$C$_y$ channel graded from $x = 0.10$ to $x = 0.40$ over 30 nm, and finally a cap layer 37 nm in thickness. An 18.5 nm oxide layer was formed by a 40 min wet thermal oxidation at 800 °C, followed by a 20 min nitrogen anneal at the same temperature. MOS capacitors were formed by deposition of an aluminum gate contact followed by a post-metal anneal at 400 °C in H$_2$/N$_2$.

Figure 1 shows the measured C(V$_G$) characteristics for this structure. Good agreement is obtained with the C(V$_G$) characteristics predicted by a one-dimensional Poisson simulator using layer parameters close to the intended ones. In particular, the characteristic “ledge” in inversion is observed, indicating that the Si$_{1-x-y}$Ge$_x$C$_y$ channel becomes inverted before the surface. The range of gate voltages over which holes are only found in the Si$_{1-x-y}$Ge$_x$C$_y$ channel is small (+0.1 > V$_G$ > -0.5 V) as this is not by any means an optimal layer structure.

**Heterostructure FET characteristics**

Heterostructure field effect transistors were fabricated using the same layer structure as in the MOS capacitor of Fig. 1. The devices were aluminum gate, non-self-aligned transistors fabricated using a 5 mask process. Subsequent to UHV/CVD growth on 7-21 ohm-cm n-type silicon (100) substrates, the source and drain regions of the MOSFETs were formed by a double boron ion implantation. The implant damage anneal was accomplished during the thermal oxidation step which was identical to that used for the MOS capacitor structure. The aluminum layer was deposited and patterned to form the gate, source and drain contacts, followed by a 365 °C forming gas anneal. Silicon surface-channel devices were also fabricated using the same process. Room-temperature characteristics of a device with $Z/L = 100$ µm /50 µm are presented in Fig.2. Well-saturated characteristics are observed with a subthreshold slope of 84 mV/decade as compared to a slope of 71 mV/decade for silicon surface-channel devices.
The field-effect mobility for holes was evaluated in two ways. As shown in Fig. 2, a plot of the channel conductance as a function of gate voltage exhibits a change in slope when holes begin to occupy the surface channel. In general, the channel conductance $G_{ch}$ of a transistor with a single channel is given by

$$G_{ch} = \mu_p \frac{Z}{L} Q_{ch} = \mu_p C_{eff} \frac{Z}{L} (V_G - V_T)$$

(1)

where $Q_{ch}$ (coul/cm$^2$) is the channel charge density, $\mu_p$ is the field effect mobility and $C_{eff}$ is the effective insulator capacitance. For small gate bias, holes are predominantly in the Si$_{1-x-y}$Ge$_x$C$_y$ channel and consequently $C_{eff}$ is given by

$$C_{eff} = \frac{1}{\frac{t_i}{\varepsilon_i} + \frac{t_{Si}}{\varepsilon_{Si}}}$$

(2)

where $t_i$ and $t_{Si}$ are the thicknesses of the SiO$_2$ insulator and the silicon cap layer and $\varepsilon_i$ and $\varepsilon_{Si}$ are the corresponding dielectric permittivities. Fitting the channel conductance (measured at $V_{DS}=0.025$) to a straight line between 0.1 and -0.5 V yields an effective mobility $\mu_p = 195$ cm$^2$/Vsec.

A more precise determination of the mobility can be made if the channel charge and channel conductance are measured directly. We measured the channel charge using the low-frequency capacitance $C_{G-SD}$ between the gate and source and drain. The measured capacitance-voltage curves are shown in Fig. 3 for both Si$_{1-x-y}$Ge$_x$C$_y$ and silicon surface-channel transistors. Measurements were performed at 10 kHz (it was verified that the same capacitance was measured at 200 Hz and 10 kHz, in order to guarantee that dispersion due to transmission-line effects$^8$ was negligible). The channel charge is then given by

$$Q_{ch} = \int_{-\infty}^{V_G} C_{G-SD}(V_G)dV_G$$

(3)

where $C_{G-SD}$ does not include the source-drain overlap capacitance. The mobility as a function of gate voltage is then obtained using eq. (1). The mobility extracted in this manner is also plotted in Fig. 3. We believe that the narrow peak near $V_G = 0.1$ V is an artifact caused by a small voltage dependence of the overlap capacitance near the onset of inversion. Apart from this artifact, a mobility of 200 cm$^2$/Vsec is observed for the Si$_{1-x-y}$Ge$_x$C$_y$ transistor for bias voltages in the range +0.1 > $V_G$ > -0.5 V. For more negative gate voltages, the mobility decreases to values typical of that for silicon surface-channel devices. For comparison, we also show the extracted mobility for a silicon surface-channel device. For this device, a peak mobility of 120 cm$^2$/Vsec is observed, which is close to but somewhat below that typically observed for silicon surface-channel devices.
Comparison with previous work

Previous work on p-channel Si_{1-x}Ge_x heterostructure transistors has shown similar mobility enhancements to those reported here. However, some of these devices used PECVD gate insulators\textsuperscript{1,3} and/or severely limited germanium content\textsuperscript{1,2,3} in the channel region. A recent study of Si_{1-x-y}Ge_xC_y heterostructure p-MOSFETs by John et al.\textsuperscript{4} used carbon to reduce the lattice strain and improve layer stability. Significantly higher (\(y = 0.007\)) carbon fractions were used compared to our work and the maximum mobility observed was not as high as that reported here.\textsuperscript{10} Similar to our work, relatively high temperatures were used for thermal oxidation and implant annealing. The reason for the discrepancy in mobility is not clear; however, there were indications that carbon had a detrimental effect on low-temperature mobility which was attributed to interface roughness. Further work is necessary to clarify the various sources of scattering and their possible dependence on carbon fraction.

The main advance in our work is the demonstration of improved carrier mobility combined with conventional gate insulator and implant annealing processes and a thick, high germanium fraction channel. This is made possible by the introduction of a small amount of carbon which reduces thermal relaxation of the strained layer. Thus mobility enhancement is obtained along with compatibility with conventional CMOS processing. We believe that a device with appropriate gate insulator and silicon cap layer thickness would offer a significant improvement in PMOS transconductance which will be highly beneficial in scaled CMOS processes.

Acknowledgements

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References

10. There is a discrepancy in [4] between a plot of the mobility and values given in the text. The correct value for the maximum mobility in a device with Si_{0.793}Ge_{0.20}C_{0.007} channel is 160 cm^2/Vsec (S. John, private communication).
Figure 1. Measured and simulated $C(V_G)$ characteristics for a heterostructure MOS capacitor (structural parameters given in text). Shown are (□) measured quasistatic capacitance; (○) measured 1 MHz capacitance, and (…….) simulated low-frequency capacitance (flatband voltage adjusted for match with measurements).
Figure 2. Measured $I_D(V_G)$ characteristics and channel conductance $G_{ch}$ for a heterostructure transistor with $Z/L = 100 \, \mu\text{m} / 50 \, \mu\text{m}$ ($V_{BS} = 0 \, \text{V}$).
Figure 3. Measured C_G-SD (open points) and extracted hole mobility (solid points) for heterostructure p-MOSFET (○,●) and silicon surface-channel MOSFET (□,■) Z/L = 100 µm /50 µm.)