Lin Li <lil53@pitt.edu>

Electrical and Computer Engineering
PhD Student
761-A Benedum Hall
Pittsburgh, PA 15261
Work: 412-624-8897 Cell: 412-913-7582

OBJECTIVE

Internship of research/engineering on computer micro-architecture, digital system design

RESEARCH INTEREST

Computer architecture, digital system IC design (ASIC, FPGA), IC reliability modeling, performance analysis, FPGA synthesis, embedded system

EDUCATION

University of Pittsburgh, Pittsburgh, PA *Sep 2007 - Present*
PhD Student in ECE Dept
- GPA: 3.97/4.0

Beihang University, Beijing, China *Sep 2005 - July 2007*
Master in EE Dept
- GPA: 3.61/4.0

Beihang University, Beijing, China *Sep 2001 - July 2005*
BS in EE Dept
- GPA: 3.73/4.0

PUBLICATIONS

- Lin Li, Youtao Zhang, Jun Yang, **"Proactive Recovery for BTI in High-k SRAM cells"**, to appear in **Design, Automation and Test in Europe (DATE)**, 2011
- Lin Li, Youtao Zhang, Jun Yang and Jianhua Zhao, **"Proactive NBTI Mitigation on Out-of-Order Function Units"**, in **Design, Automation and Test in Europe (DATE)**, pp. 411-416, 2010
- Lin Li, Xiuyi Zhou, Jun Yang and Victor Puchkarev, **"ThresHot: An Aggressive Task Scheduling Approach in CMP Thermal Design"**, in workshop on **Unique Chips and Systems (UCAS-05)** with **IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS)**, 2009
- Lin Li, Xi Yang, Xiaolin Zhang, **"Embedded Platform Construction and Performance Test Based on LEON Soft-Core"**, in **Microcontroller & Embedded Systems**, pp. 32-35, Jan 2007

RESEARCH PROJECTS

- **PBTI and NBTI Reliability Improvement on High-k based SRAM cells**
  With the high-k metal gate technology under 45nm, PBTI on NMOS and NBTI on PMOS cause severe reliability problems for SRAM cells. This work models and analyzes the impact of BTI on read, write and access time failures of SRAM cells by Monte-Carlo Hspice simulations. The proposed novel proactive recovery scheme effectively recovers 4 transistors in a 6T SRAM cell of the bank under recovery mode, resulting extended lifetime for SRAMs. Statistical methods are used in R for accurate life time evaluation, and a Perl script is used to generate and run the sample simulations.
- **NBTI Reliability Improvement on OoO Function Units**

This work explores the opportunity and improvement of applying proactive recovery technique to the Out-of-Order units in microprocessor. The accuracy of timing model in the SimpleScalar simulator is substantially enhanced with register renaming support and independent Integer and Floating-Point units. With carefully designed entry-level controller, abundant idle cycles are explored to apply proactive recovery, which extends the lifetime of OoO units by average of 5X.

- **Thermal Aware Scheduling on Chip-Multiprocessor**
  This work studies the thermal behavior of the running multiple workloads on Chip Multiprocessor with DVFS, and the tradeoff between thermal behavior and performance. The proposed online ThresHot algorithm schedules the workloads such that least DVFS events are triggered for improving performance, based on gathered information of dynamic temperature of cores and power of workloads. Comparing to Round-Robin and others, ThresHot achieves best performance and eliminates unnecessary workloads schedulings. The algorithm is implemented in Perl, which runs as a children process forked by Hotspot simulator (written in C) process with inter-process communication.
- **Embedded System Prototype Board Design**
  The embedded system based on Freescale ARM9 CPU is designed and built for a lab class. The schematic and PCB layout are implemented in Cadence Allegro. In this 6-layer PCB design, the CPU communicates with the SDRAM, LCD controller, UART port and other interfaces. The bootloader, Linux 2.4 kernel and root file system are then ported to the hardware to support application development on embedded system.

COURSE PROJECTS

- **Computer Architecture**
  Simics simulator is extensively used to study the influence of computer architecture on program performance. The projects include: measuring performance of programs with varying size of working set in cache, extracting histogram of branch distances and distinct basic blocks, designing programs to measure the cache parameters, and designing a malicious program to extensively stress the shared memory and slow down the performance of programs on 8-core Niagara T1 processor. C is extensively used.
- **VLSI Design and Layout**
  An 32bit ALU with register file is implemented with the tsmc 0.18μ process with 6 metal layers in Cadence Virtuoso. All the function components, including adder, shifter and register files with decoders are custom designed as well as the interconnection. The final layout takes only 3 metal layers with optimized delay and power consumption. Final layout for manufacturing is also generated.
- **Advanced SoC Design**
  A cache coherence protocol (MESI) controller is implemented for the L2 cache shared by two OpenRISC 1200 cores. The controller tracks and updates the state of each cache line when monitoring the messages on the snooping bus. The design is implemented and synthesized in Synopsys Design Compiler, and placed and routed in Cadence Encounter. The LEF file is also modified to accommodate the custom designed memory macro in work flow. The function and final timing are verified as specification.
- **Compiler Design**
  Lex, Yacc, and C are extensively used to build the front end and code generation part of a compiler for mini-Java language. The front end includes the Lex specification for token generation, the Yacc rules to build the syntax tree and semantic check rules to detect semantic errors. The code generation part translates the syntax tree and symbol table into a program

in MIPS assembly language, which is verified in SPIM simulator.

- **VGA Controller and Driver Support on Xilinx FPGA**
  A VGA controller is designed to enable the powerpc405 core in Virtex4 FPGA to generate display on VGA monitor. The controller takes advantage of the fast built-in BRAM to cache the image data from the high-speed PLB bus. Also the driver to configure and use the controller is developed to support the port of Doom game on Virtex4 FPGA.

PH.D. COURSE

ECE2120 Hardware Design Methodology, ECE2192 Introduction to VLSI, ECE2193 Advanced VLSI Design, CS2150 Design and Analysis of Algorithms, CS2410 Computer Architecture, ECE2140 SoC Design, CS2310 Software Engineering, CS2210 Compiler Design

WORK EXPERIENCE

Graduate Research/Teaching Assistant *Sep 2007 - Present*
Dept of ECE, University of Pittsburgh

Summer Internship in HK Polytechnic University *Jul 2006 - August 2006*
Industry Center, Hong Kong Polytechnic University

TEACHING EXPERIENCE

From Fall 2007 I have been a teaching assistant in 3 undergraduate courses with multiple sessions: Digital Lab, Introduction to Computer Networks, Computer Organization. In lab course, I am responsible for assisting students with lab problems in building circuits on bread boards and using equipments such as oscilloscope, logic analyzer and FPGA board. In lecture course, I am responsible for holding recitation sessions as well as grading assignments. I was awarded best teaching assistant of CoE in 2009.

AWARD AND MEMBERSHIP

- Best teaching assistant in CoE Dept, University of Pittsburgh, Mar 2009
- First Prize of Intel Cup Embedded System Design Contest, Shanghai, China, Oct 2004
- First Prize of Science and Technology Contest, Beihang University, China, Mar 2004
- First Prize of Physics Contest, Beijing, China, Dec 2002
- First Prize of Mathematics Contest, Beijing, China, Dec 2002
- IEEE student member since 2009

TECHNICAL SKILLS

- Micro-Arch Simulators: Simics, SimpleScalar, PTLSim, HotSpot. Proficiently developing customized modules and enhancing the processor models for research.
- Basic programming languages: 6 years experience of C/C++, Matlab. Efficiently developing models with libraries and toolboxes.
- Hardware design languages: Verilog, VHDL. Efficiently implementing, verifying small to medium scale digital systems.
- Digital Design Flow: Cadence Virtuoso & Encounter, Synopsis Design Compiler, Hspice & PrimeTime, Mentor Modelsim, Xilinx ISE, Altera Quartus. Very familiar with ASIC and FPGA synthesizing, placing and routing, functional and timing verification, and customized layout.
- Script languages: 5 years experience of Perl, Linux Bash Shell script to automate the tasks in Linux.
- 5 years Unix/Linux experience, including application development for embedded systems and system administration.