# Program Interference in MLC NAND Flash Memory: Characterization, Modeling, and Mitigation

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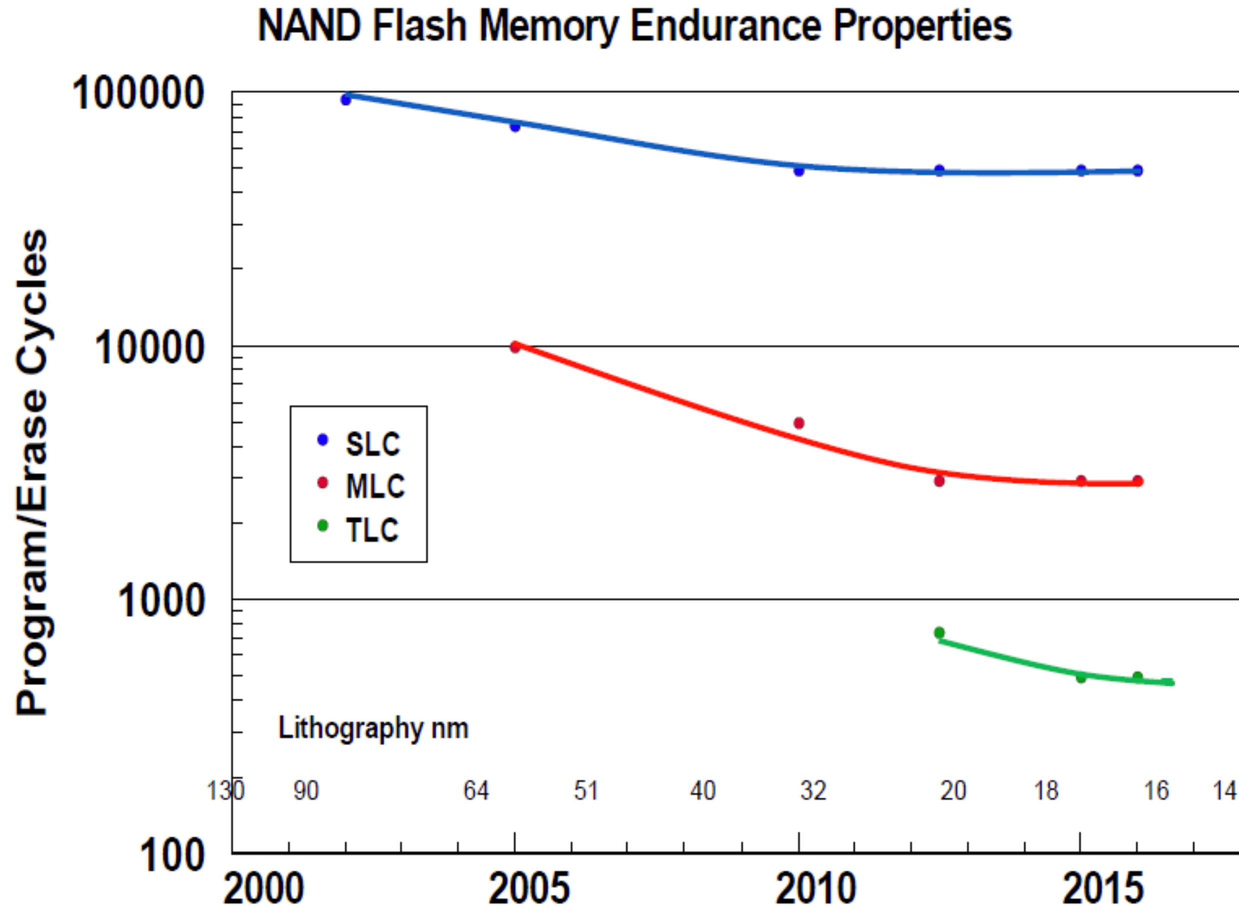
# Flash Challenges: Reliability and Endurance




E. Grochowski et al., "Future technology challenges for NAND flash and HDD products", Flash Memory Summit 2012

- **P/E cycles (provided)**

**A few thousand**

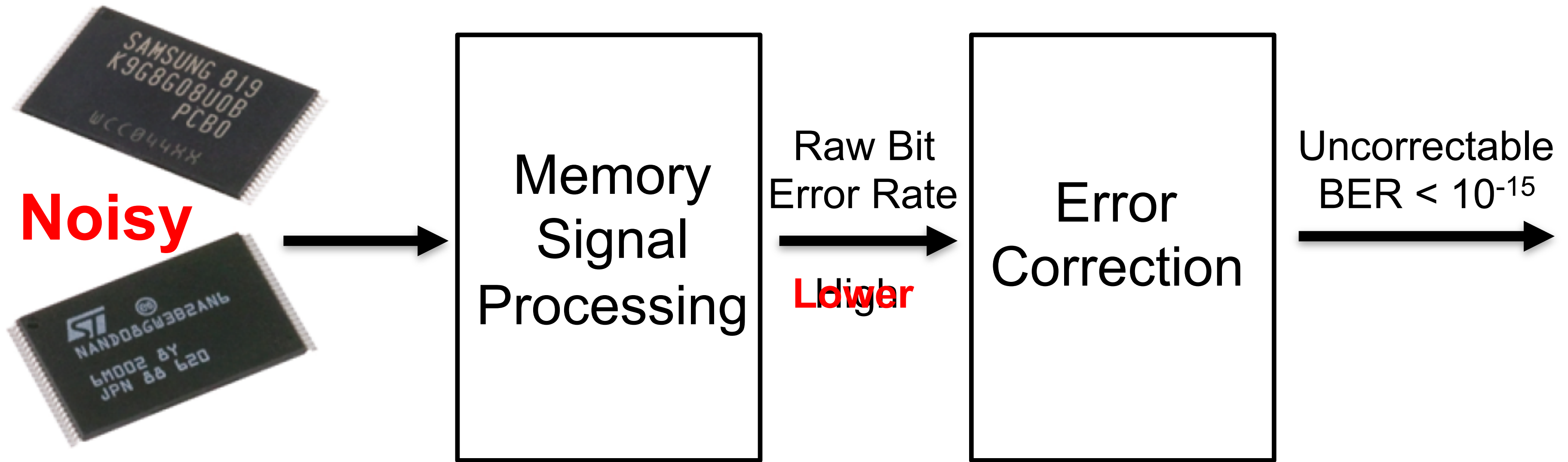
- **P/E cycles (required)**

Writing
the full capacity
of the drive
10 times per day
for 5 years
(STEC)

**> 50k P/E cycles**

# NAND Flash Memory is Increasingly Noisy

# Future NAND Flash-based Storage Architecture



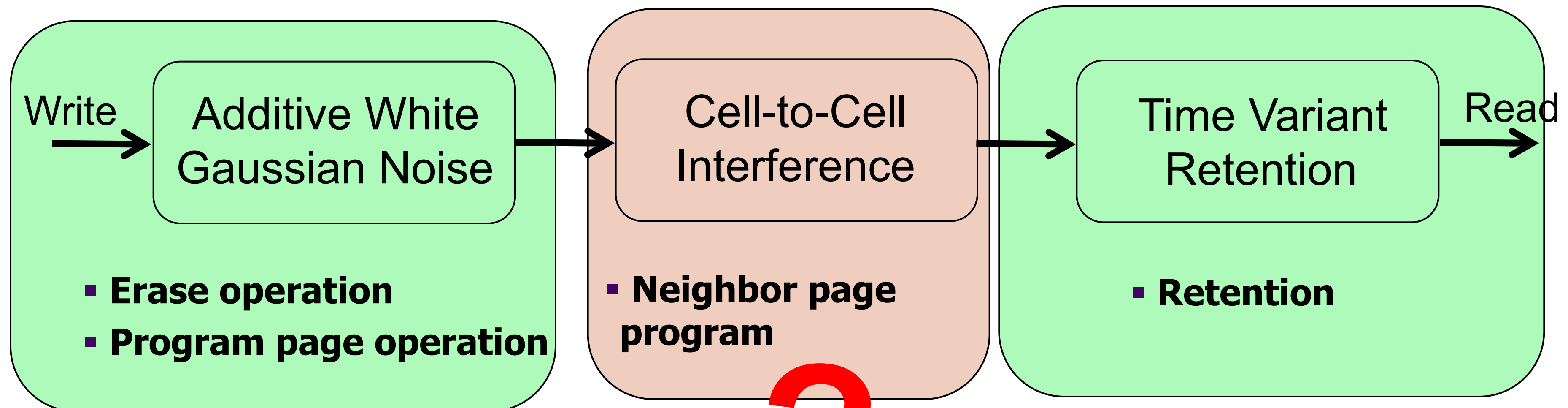

Our Goals:

Model NAND Flash as a digital communication channel

Design efficient reliability mechanisms based on the model

# NAND Flash Channel Model

Simplified NAND Flash channel model based on dominant errors




Cai et al., "Threshold voltage distribution in MLC NAND Flash Memory: Characterization, Analysis, and Modeling", DATE 2013

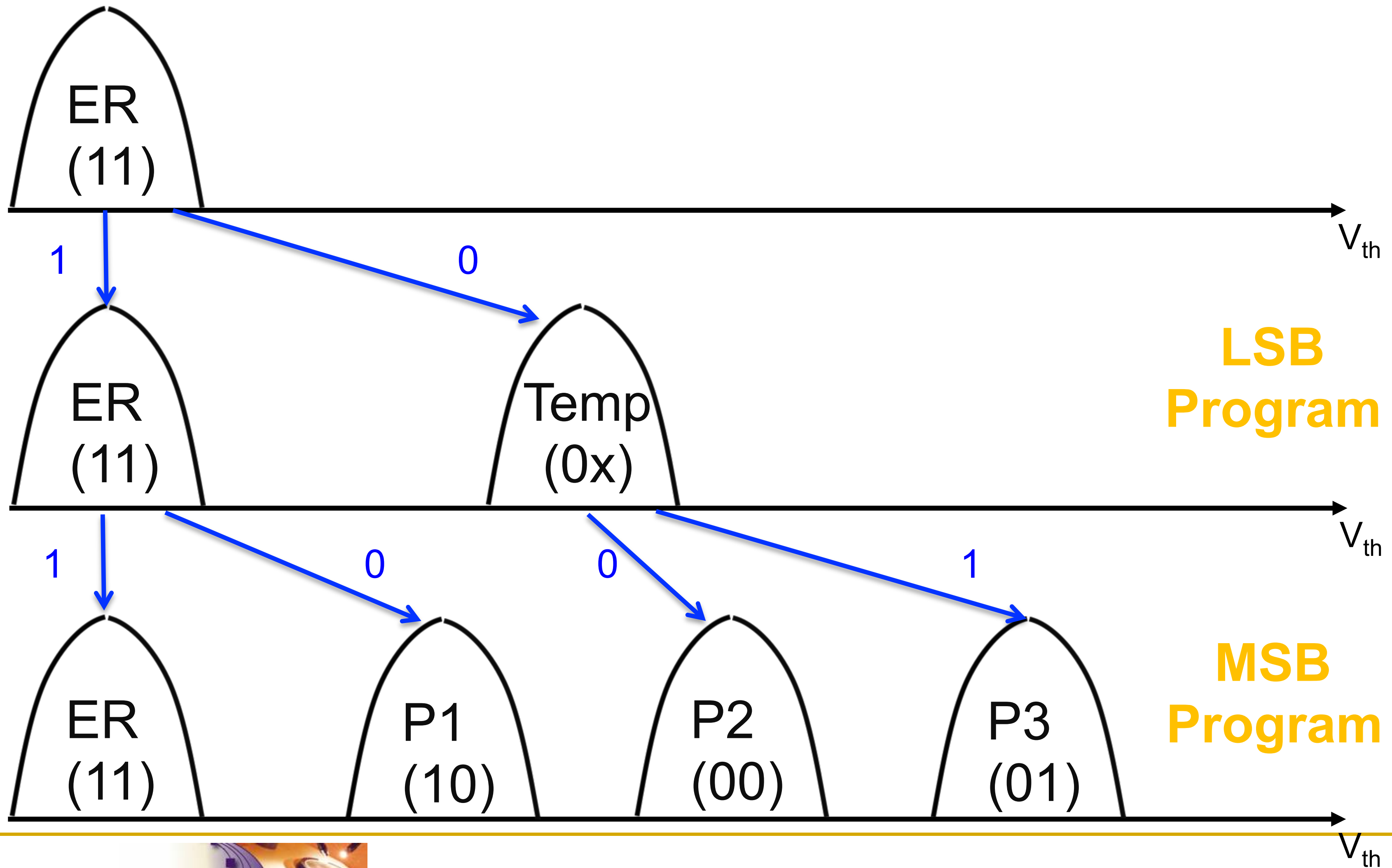
Cai et al., "Flash Correct-and-Refresh: Retention-aware error management for increased flash memory lifetime", ICCD 2012

# Outline

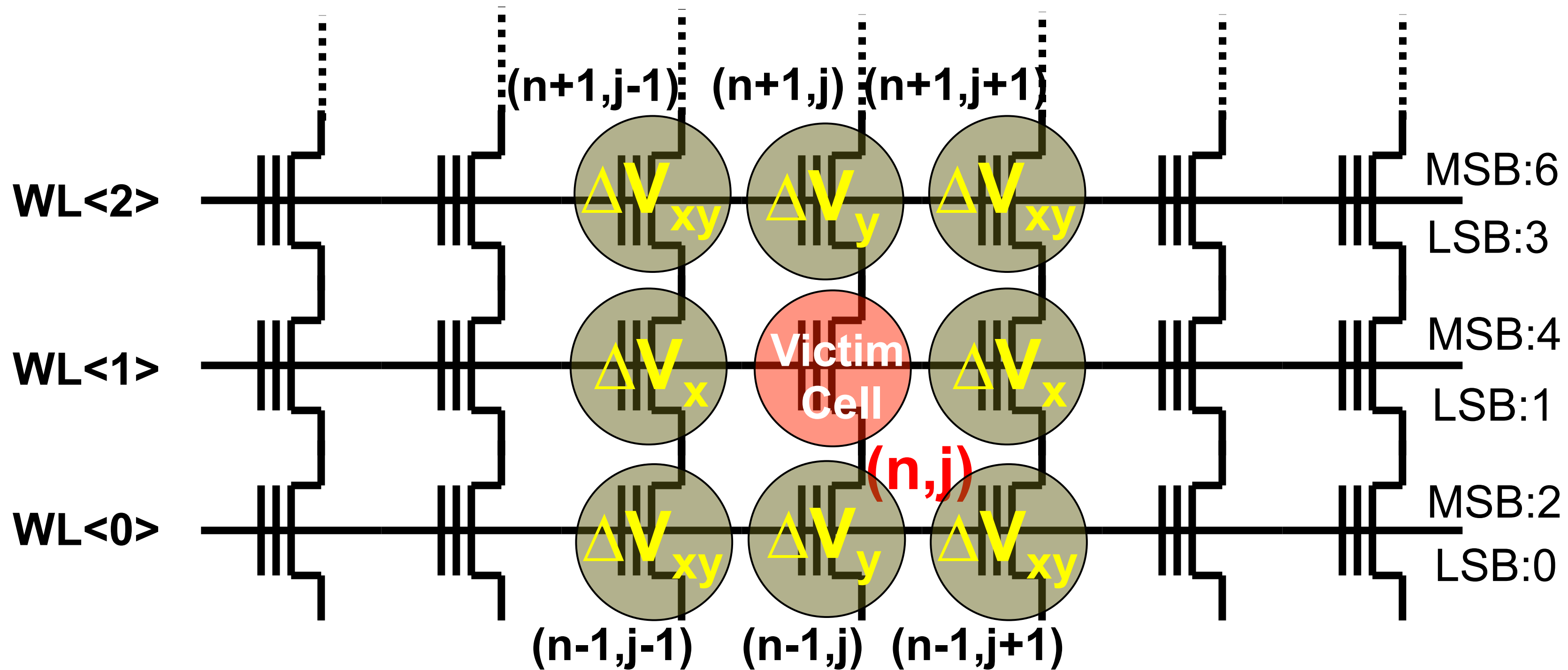
- Background on Program Interference
- Characterization of Program Interference
- Modeling and Predicting Program Interference
- Mitigation of Program Interference
  - Read Reference Voltage Prediction
- Conclusions

# How Current Flash Cells are Programmed

- Programming 2-bit MLC NAND flash memory in two steps



# Basics of Program Interference




- Traditional model of victim cell threshold voltage changes when neighbor cells are programmed

$$\Delta V_{victim} = (2C_x \Delta V_x + C_y \Delta V_y + 2C_{xy} \Delta V_{xy}) / C_{total}$$

# Previous Work Summary

- No previous work **experimentally** characterized and modeled threshold voltage distributions under program interference

- Previous modeling work
  - *Assumes* linear correlation between the program interference induced threshold voltage change of the victim cell and the threshold voltage changes of the aggressor cells
  - Coupling capacitance and total capacitance of each flash cell are the key coefficients of the model, which are process and design dependent random variables
  - Their exact capacitance values are difficult to determine
  - Previously proposed model cannot be realistically applied in flash controller

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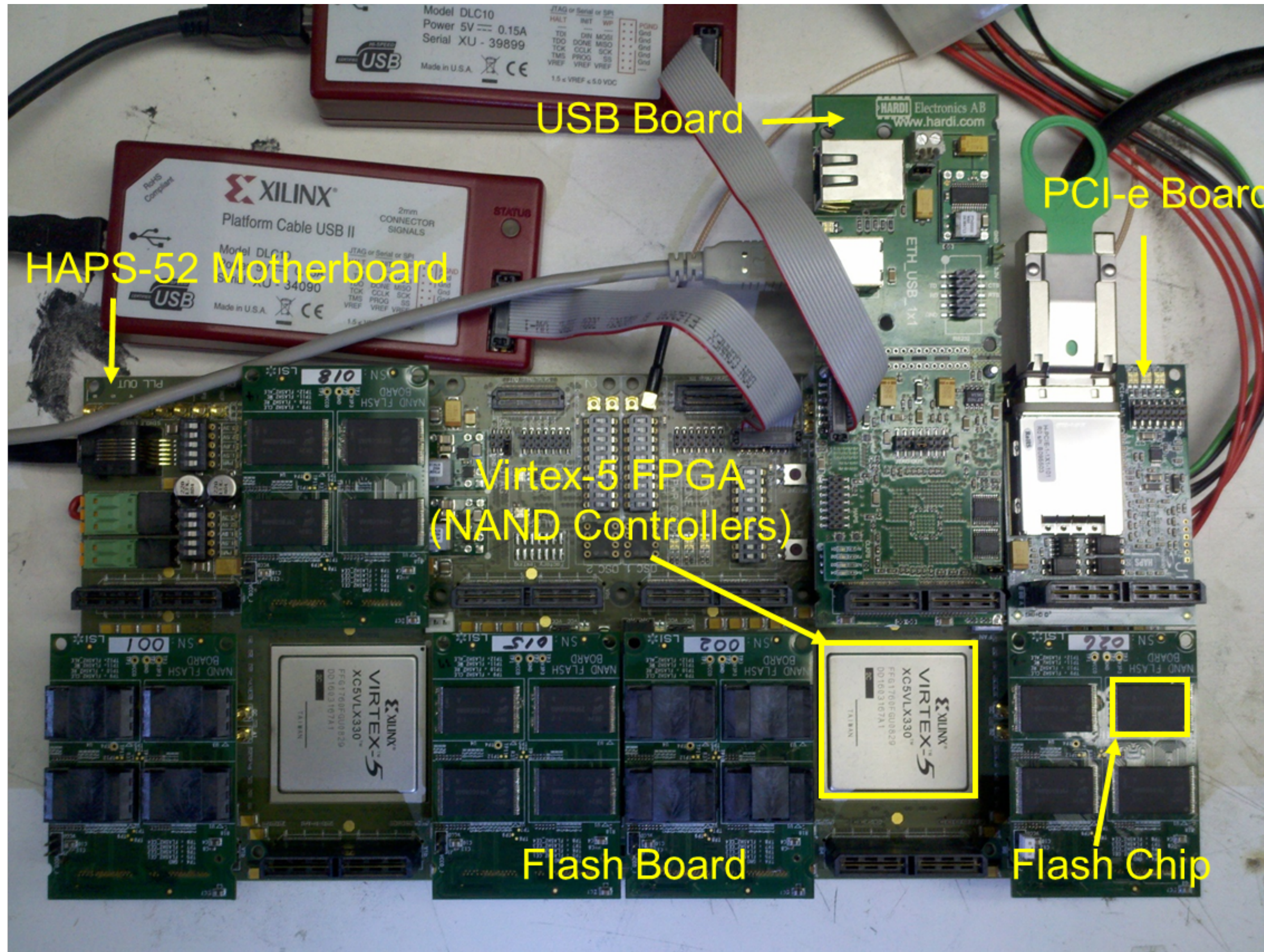
# Characterization Hardware Platform

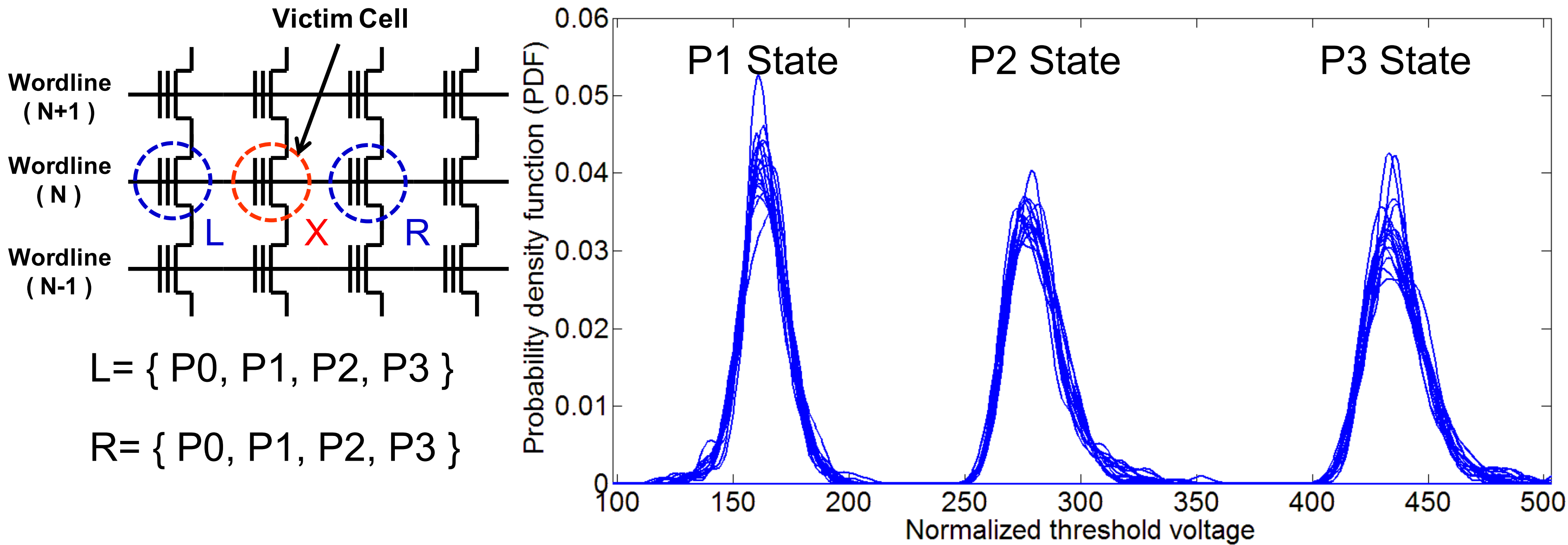



Cai et al., “FPGA-Based Solid-State Drive Prototyping Platform”, FCCM 2011

# Characterization Studies

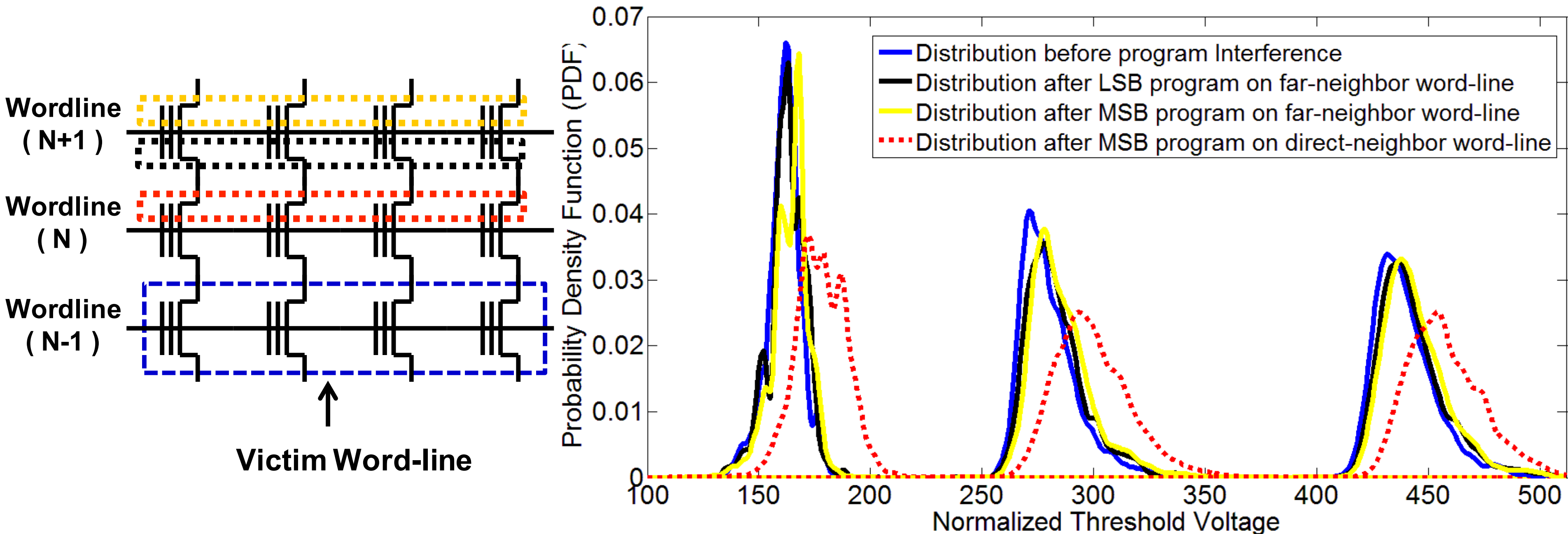
- Bitline to bitline program interference
- Wordline to wordline program interference
  - Program in page order
  - Program out of page order

# Bitline to Bitline Program Interference



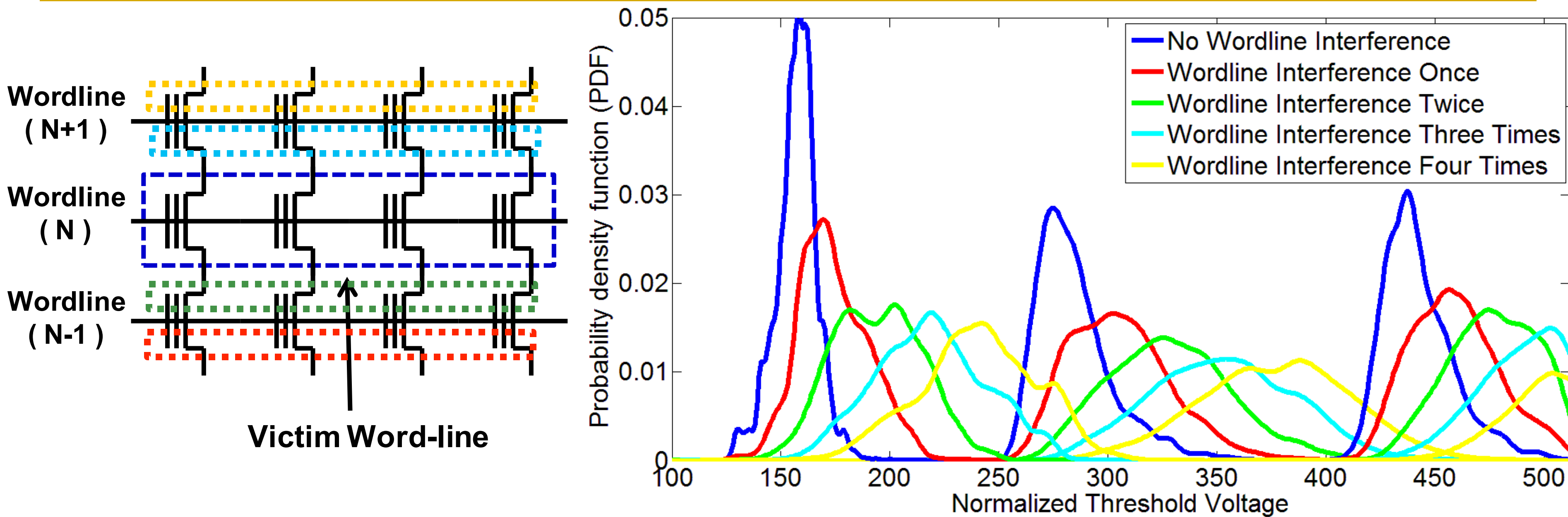

- $V_{th}$ distributions of victim cells under 16 ( 4 x 4) different neighbor values {L, R} almost overlap
- Bitline to bitline program interferences are small

# WL to WL Interference with In-Page-Order Programming




- Program interference increases the threshold voltage of victim cells and causes threshold voltage distributions shift to the right and become wider
- Program interference depends on the locations of aggressor cells in a block
  - Direct neighbor wordline program interference is the dominant source of interference
  - Neighbor bitline and far-neighbor wordline interference are orders of magnitude lower

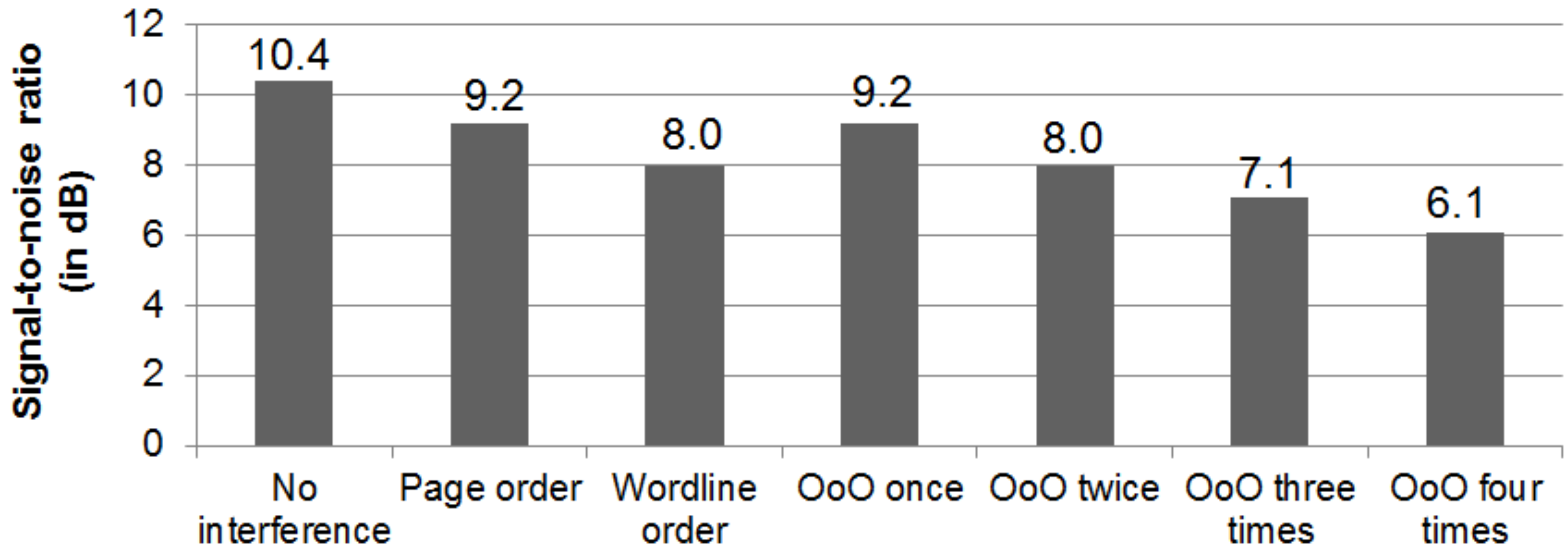
# WL to WL Interference with Out-of-Page-Order Programming




- The amount of program interference depends on the programming order of pages in a block
  - In-page-order programming likely causes the least amount of interference
  - Out-of-page-order programming causes much more interference

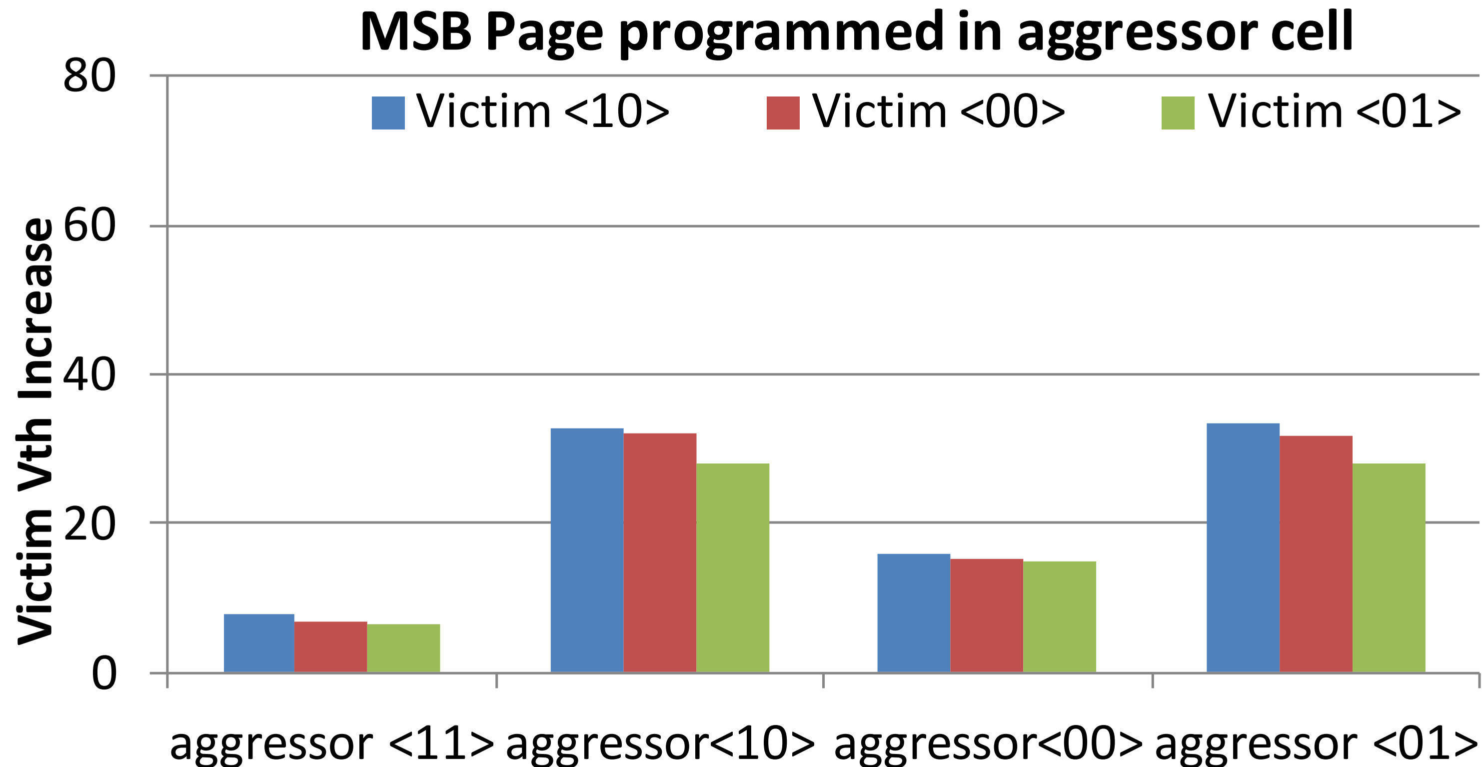
# Comparison under Various Program Interference

- Signal-to-noise ratio comparison




**Out-of-page-order Programming**

# Data Value Dependence of Program Interference




- The amount of program interference depends on the values of both the aggressor cells and the victim cells

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# Linear Regression Model

- Feature extraction for $V_{th}$ changes based on characterization
  - Threshold voltage changes on aggressor cell
  - Original state of victim cell

- Enhanced linear regression model

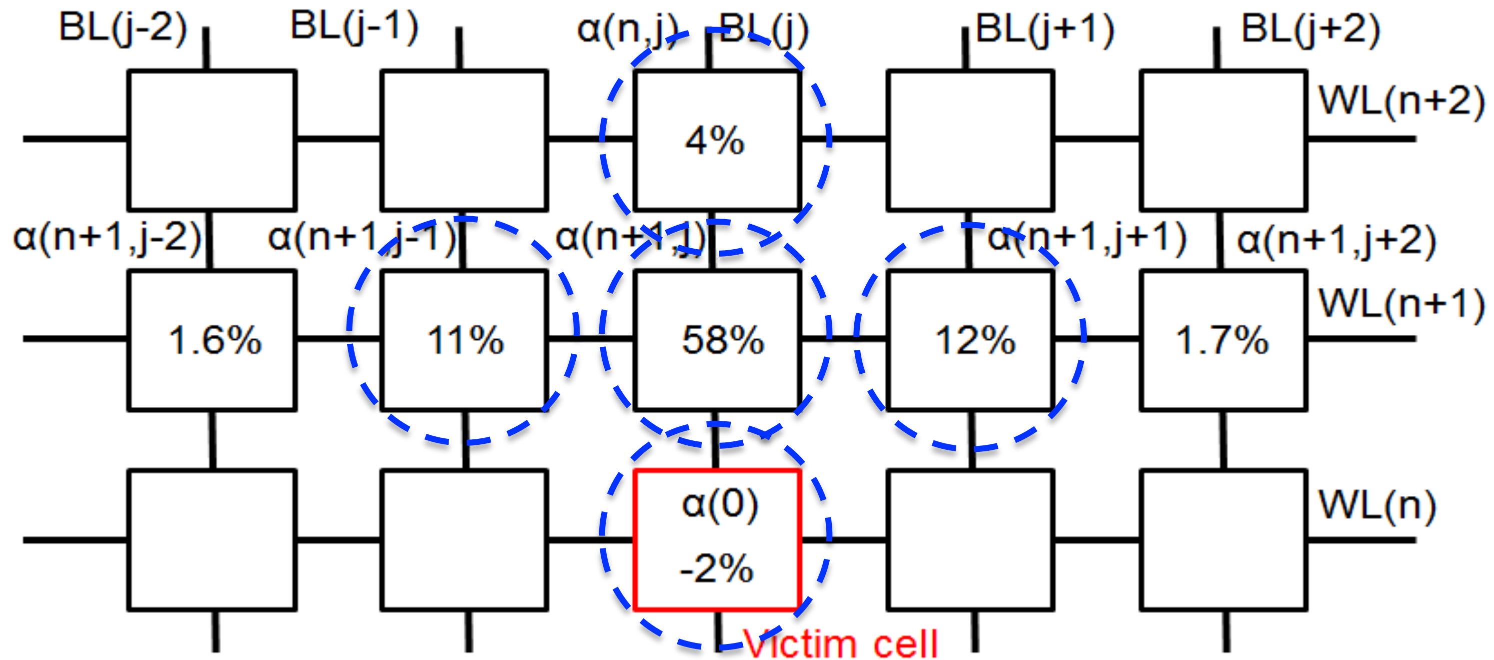
$$\Delta V_{victim}(n,j) = \sum_{y=j-K}^{j+K} \sum_{x=n+1}^{n=M} \alpha(x,y)\Delta V_{neighbor}(x,y) + \alpha_0 V_{victim}^{before}(n,j)$$

$$Y = X\alpha + \varepsilon$$ (vector expression)

- Maximum likelihood estimation of the model coefficients

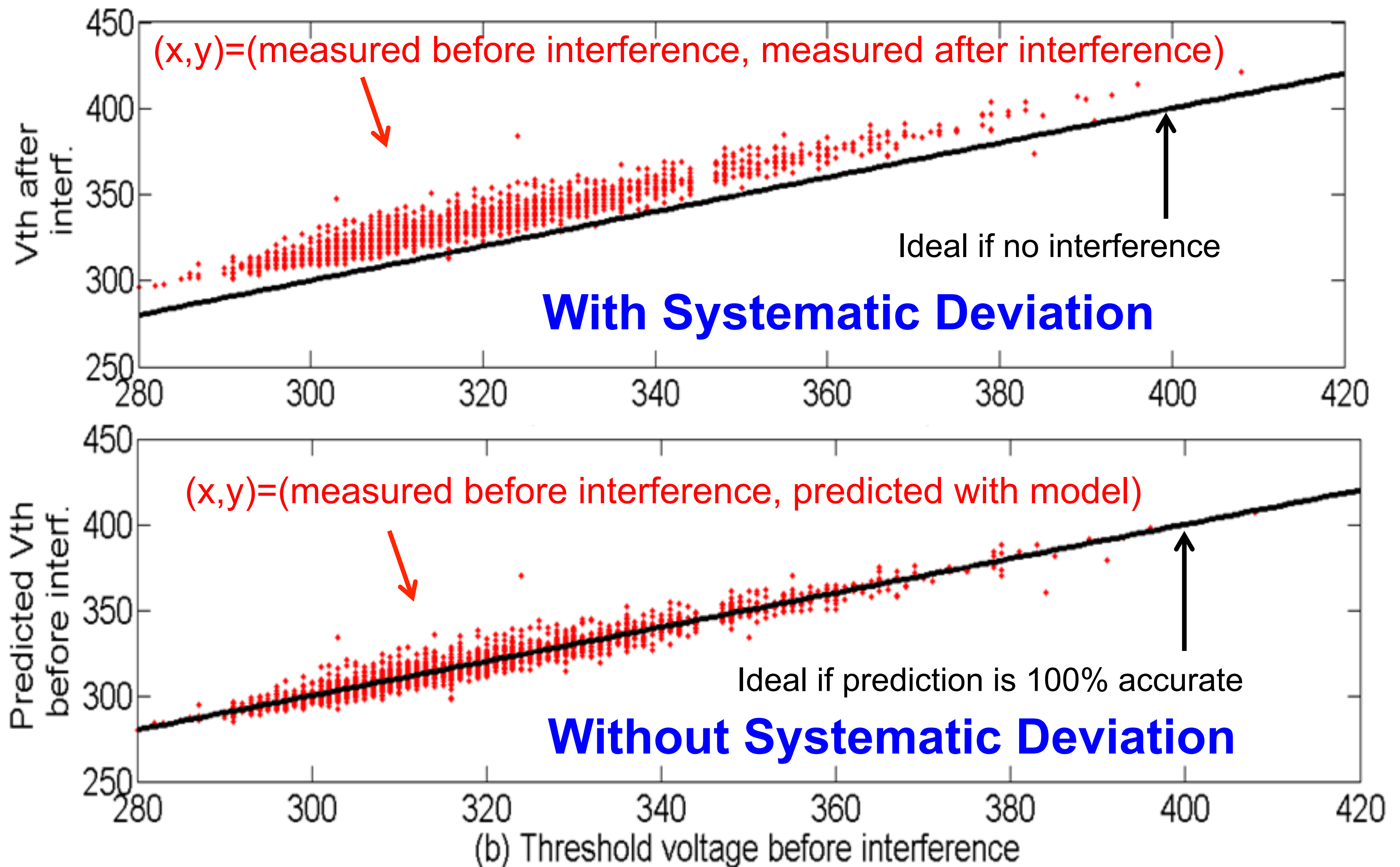
$$\arg\min_{\alpha}(\|X \times \alpha - Y\|_2^2 + \lambda\|\alpha\|_1)$$

# Model Coefficient Analysis

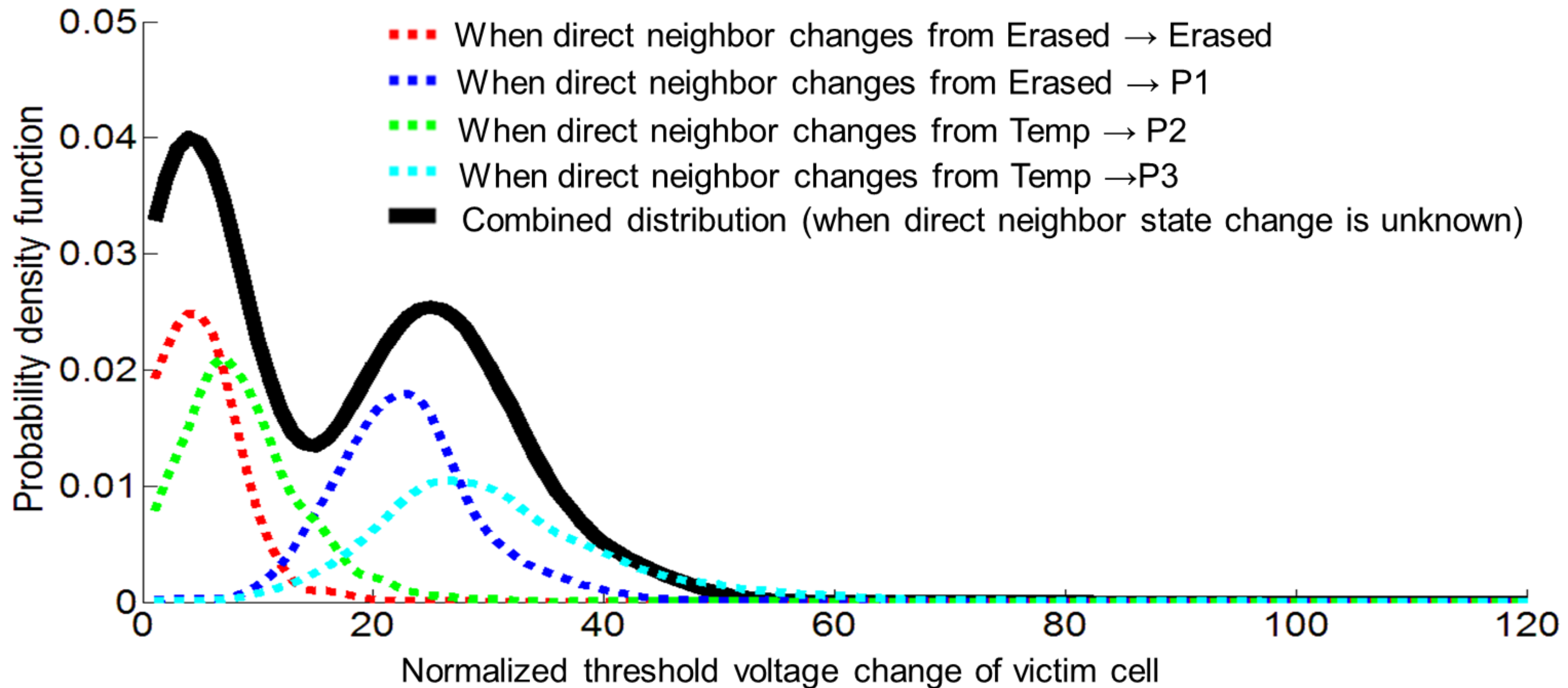



- Direct above cell dominance
- Direct diagonal neighbor second
- Far neighbor interference exists
- Victim cell's Vth has negative affect

# Model Accuracy Evaluation

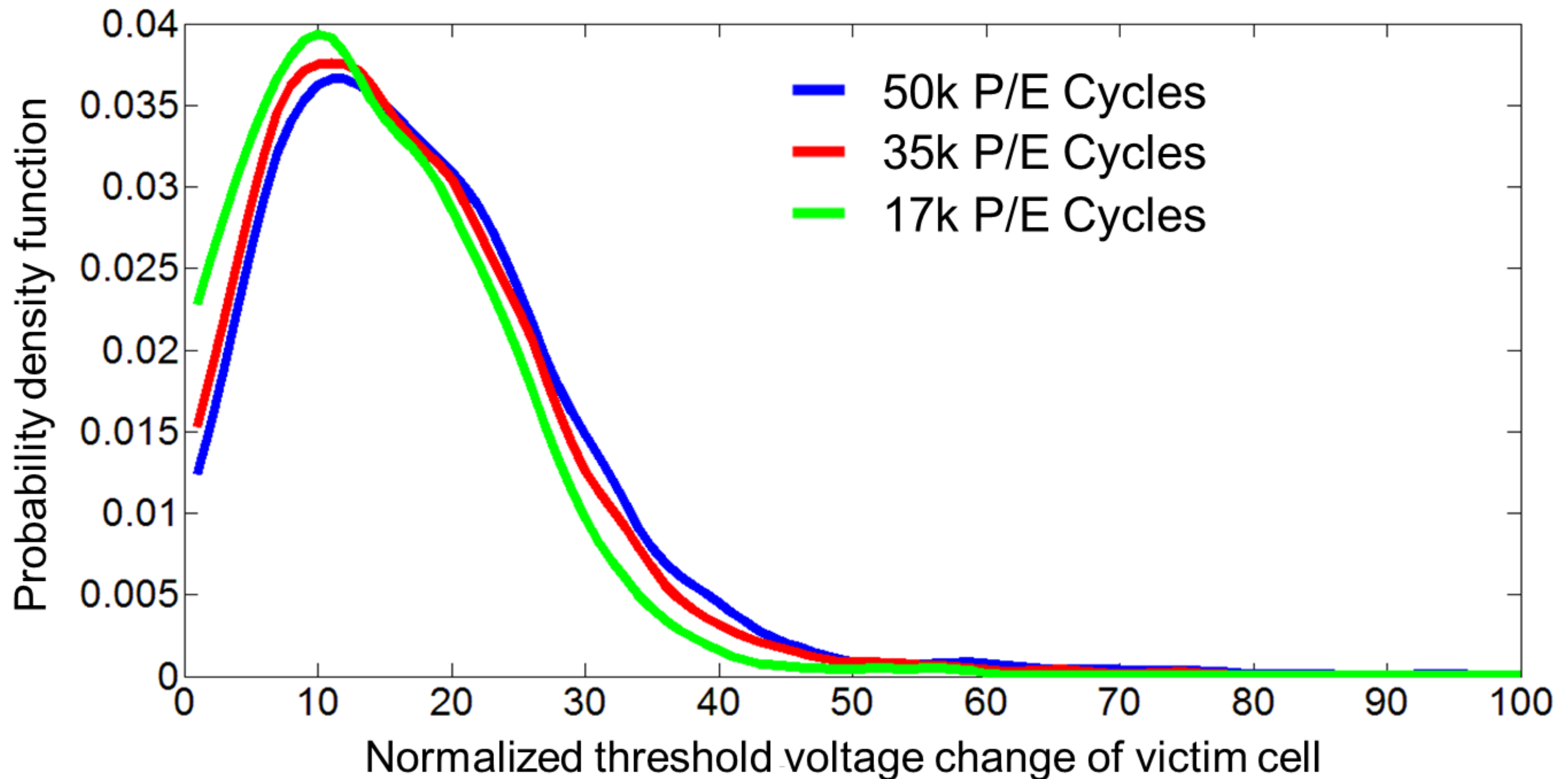


# Distribution of Program Interference Noise




- Program interference noise follows multi-modal Gaussian-mixture distribution

# Program Interference vs P/E Cycles




- Program interference noise distribution does not change significantly with P/E cycles

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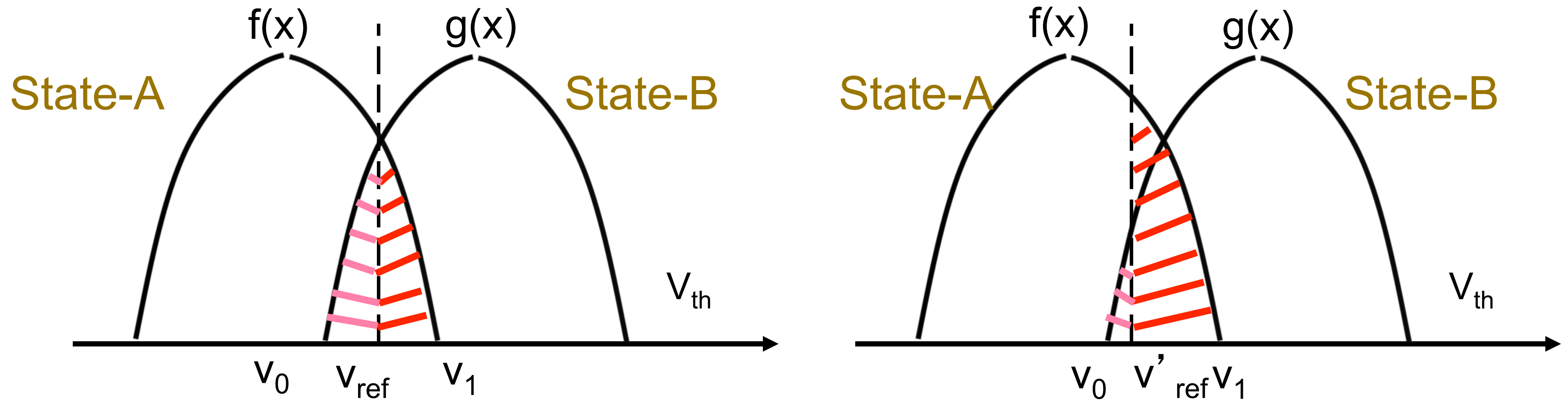
# Optimum Read Reference for Flash Memory

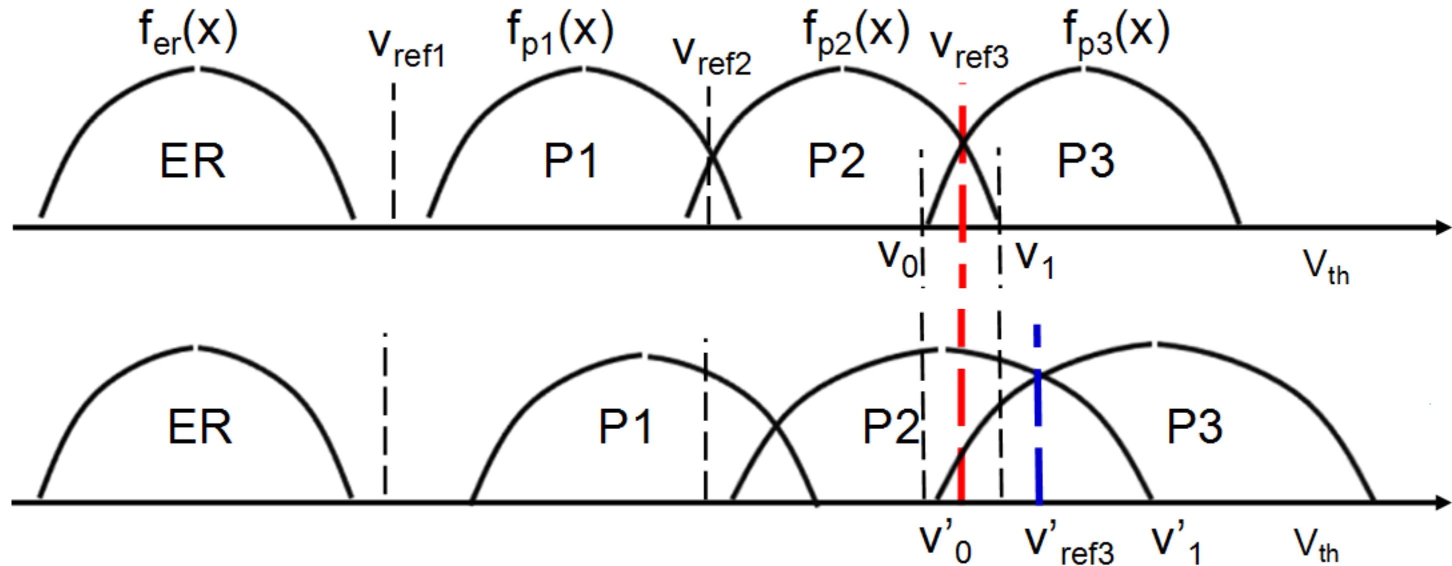
- Read reference voltage can affect the raw bit error rate




$$BER1 = \int_{v_{ref}}^{+\infty} f(x)dx + \int_{-\infty}^{v_{ref}} g(x)dx \qquad BER2 = \int_{v'_{ref}}^{+\infty} f(x)dx + \int_{-\infty}^{v'_{ref}} g(x)dx$$

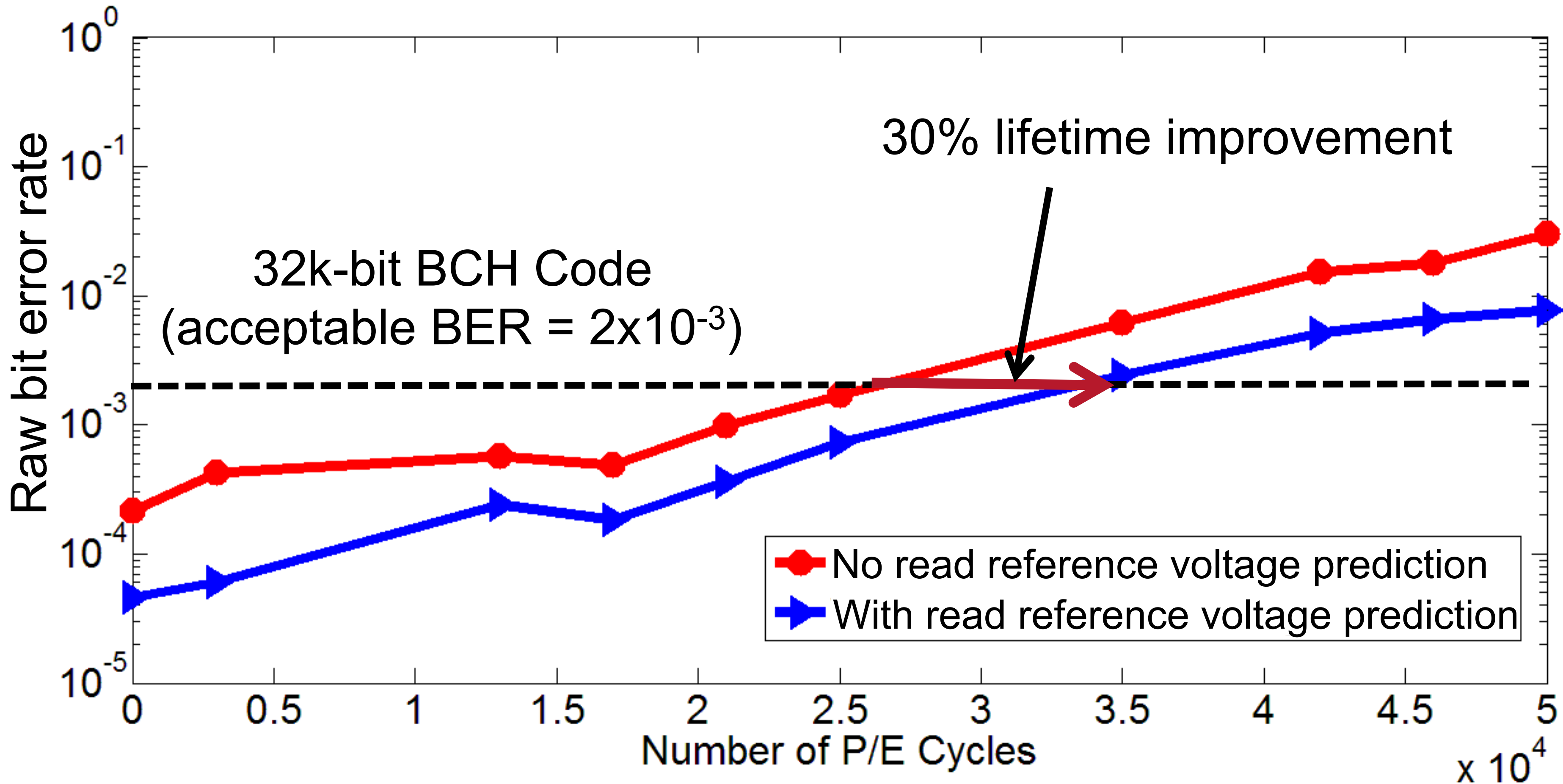
- There exists an optimal read reference voltage
  - Predictable if the statistics (i.e. mean, variance) of threshold voltage distributions are characterized and modeled

# Optimum Read Reference Voltage Prediction




- Learning function (periodically, every ~1k P/E cycles)
  - Program known data pattern and test Vth
  - Program aggressor neighbor cells and test victim Vth after interference
- Optimum read reference voltage prediction
  - Default read reference voltage + Program interference noise mean

# Evaluation Results




- Read reference voltage prediction can reduce raw BER and increase the P/E cycle lifetime

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# Key Findings and Contributions

- Methodology: Extensive experimentation with real 2Y-nm MLC NAND Flash chips

- Amount of program interference is dependent on
  - Location of cells (programmed and victim)
  - Data values of cells (programmed and victim)
  - Programming order of pages

- Our new model can predict the amount of program interference with 96.8% prediction accuracy

- Our new read reference voltage prediction technique can improve flash lifetime by 30%

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