The University of Texas at Austin
Electrical and Computer Engineering
Cockrell School of Engineering

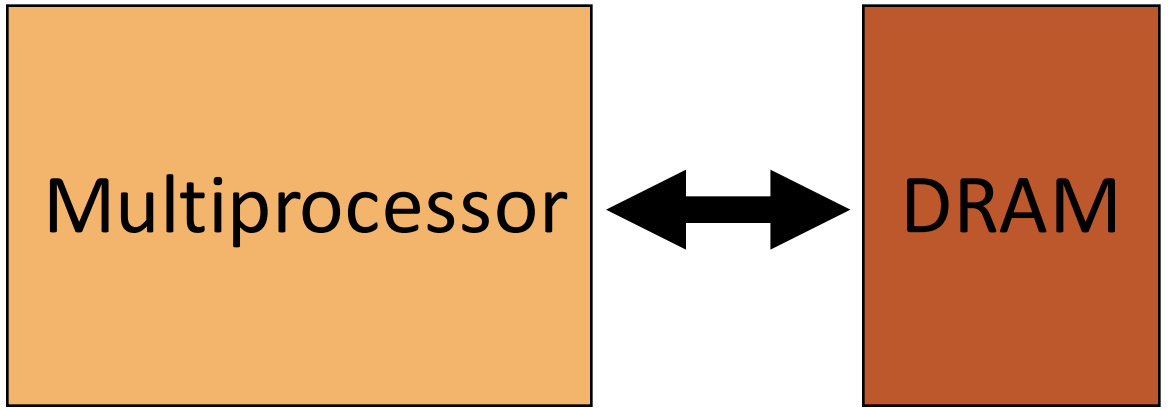
Accelerating Dependent Cache Misses with an Enhanced Memory Controller

Milad Hashemi, Khubaib, Eiman Ebrahimi, Onur Mutlu, Yale N. Patt

Tuesday June 21: Session 7A, 3:30pm

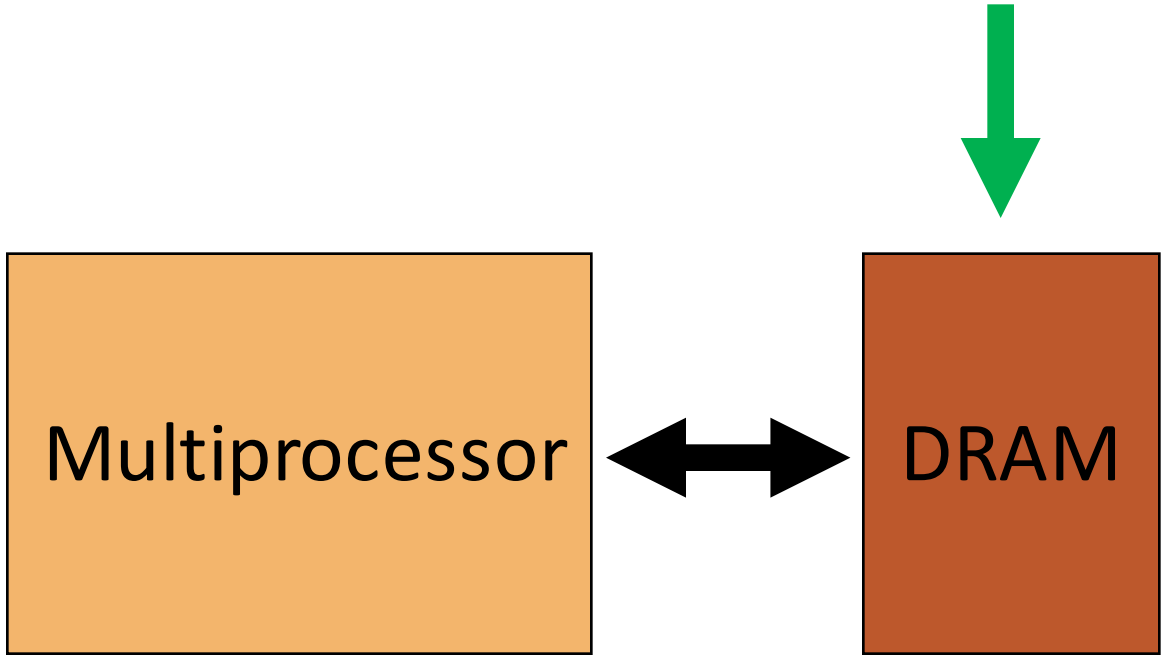
Memory Access Latency

- The latency of accessing main memory is made up of two parts:



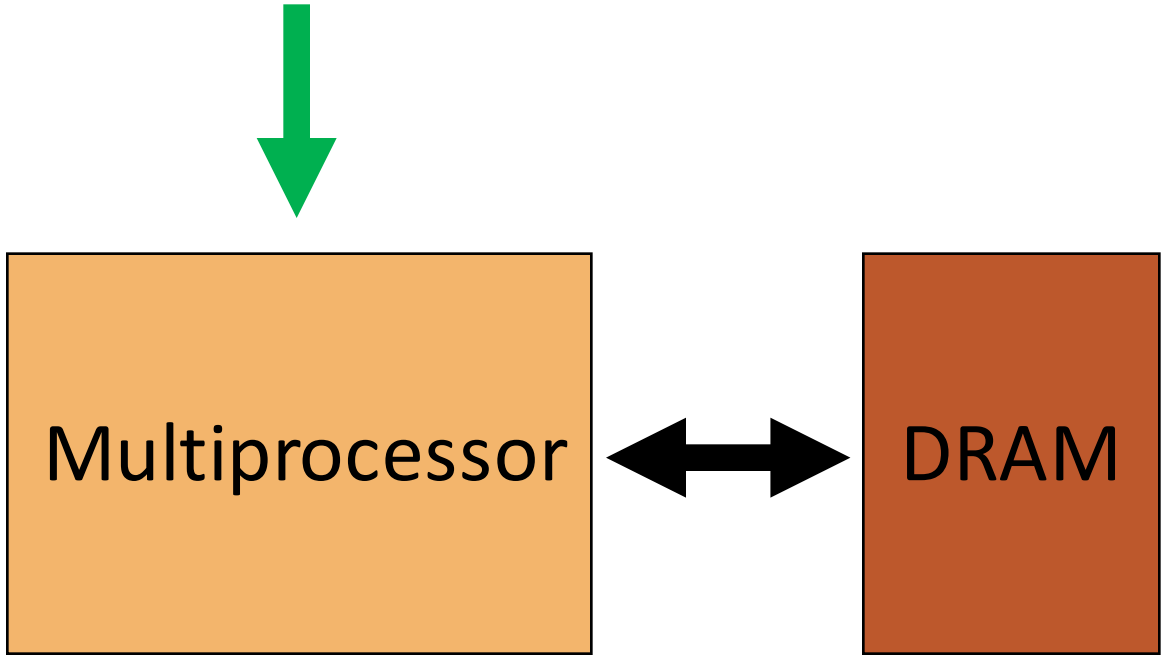
Memory Access Latency

- The latency of accessing main memory is made up of two parts:
  - DRAM access latency

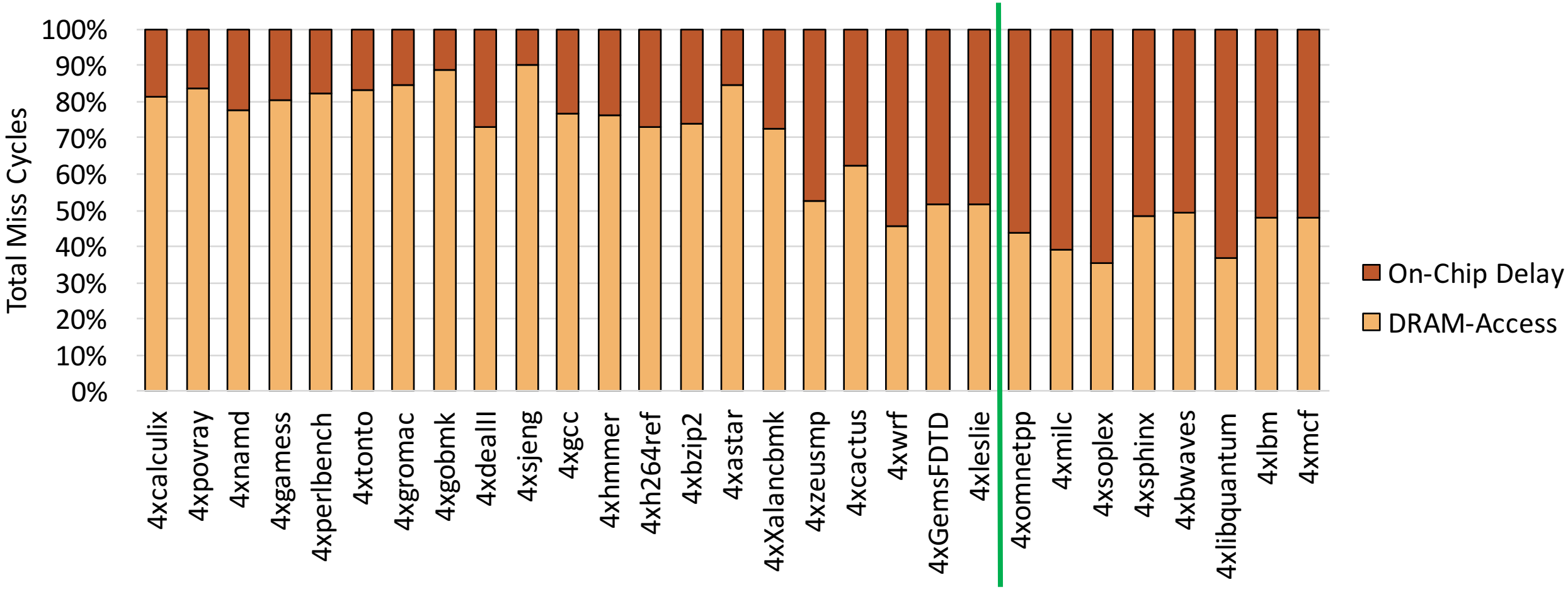


Memory Access Latency

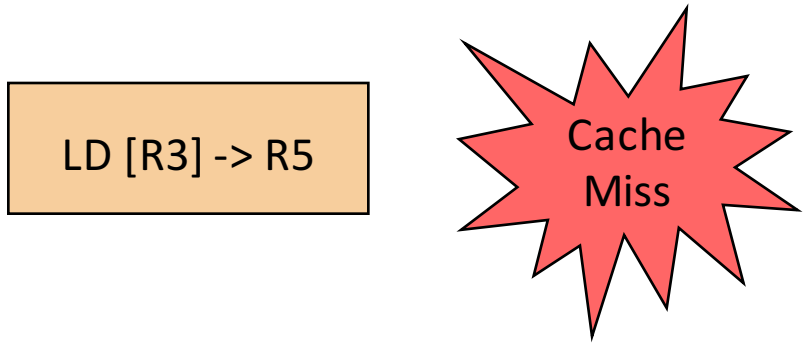
- The latency of accessing main memory is made up of two parts:
  - DRAM access latency
  - On-chip latency



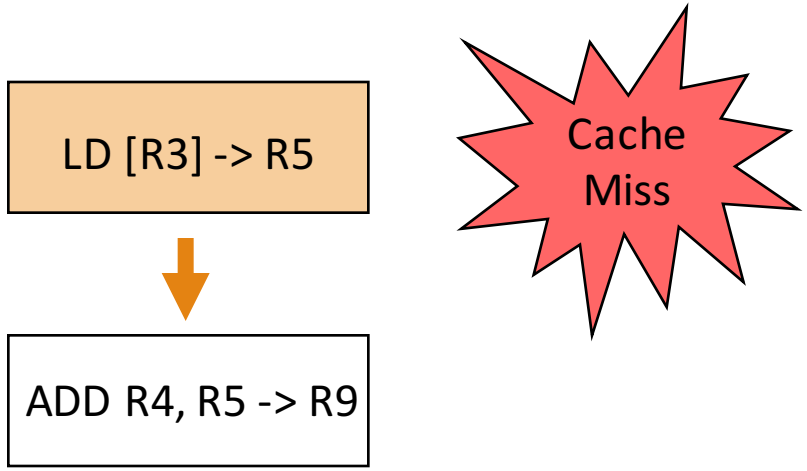
On-Chip Delay



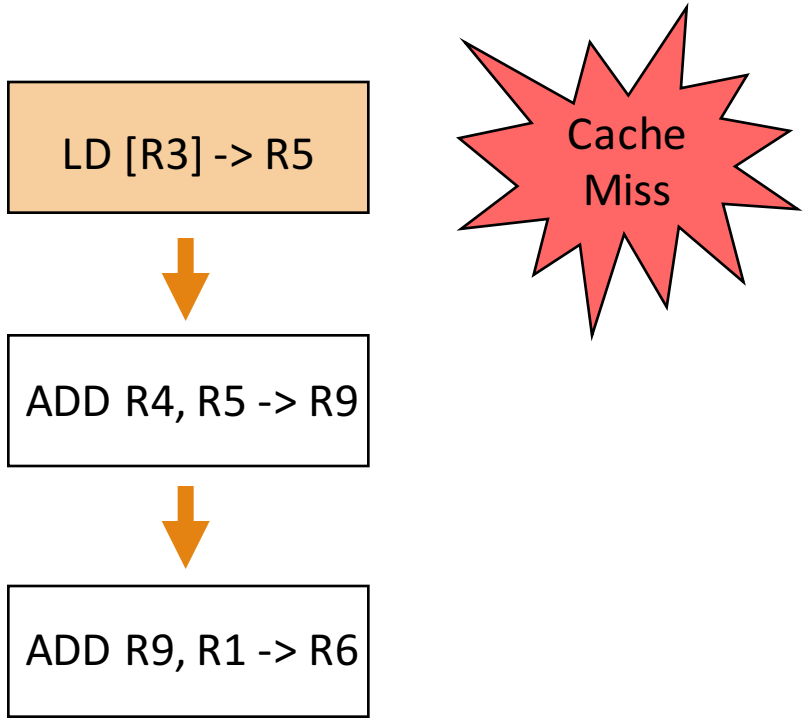
Dependent Cache Misses



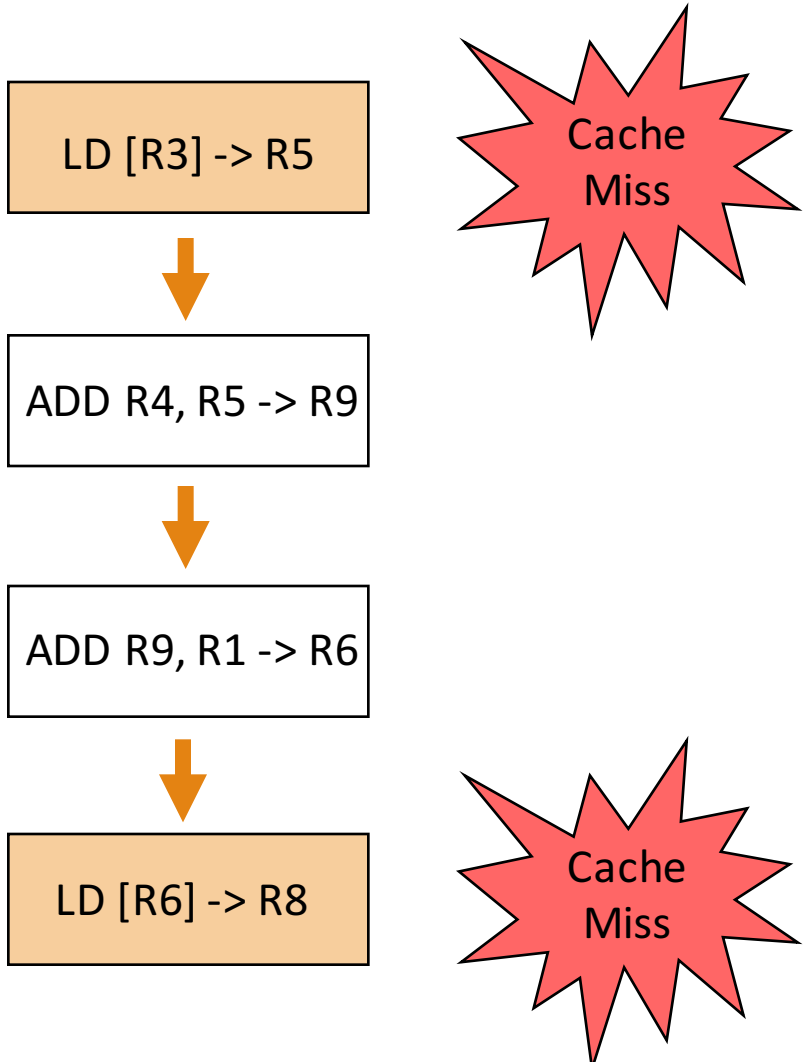
Dependent Cache Misses



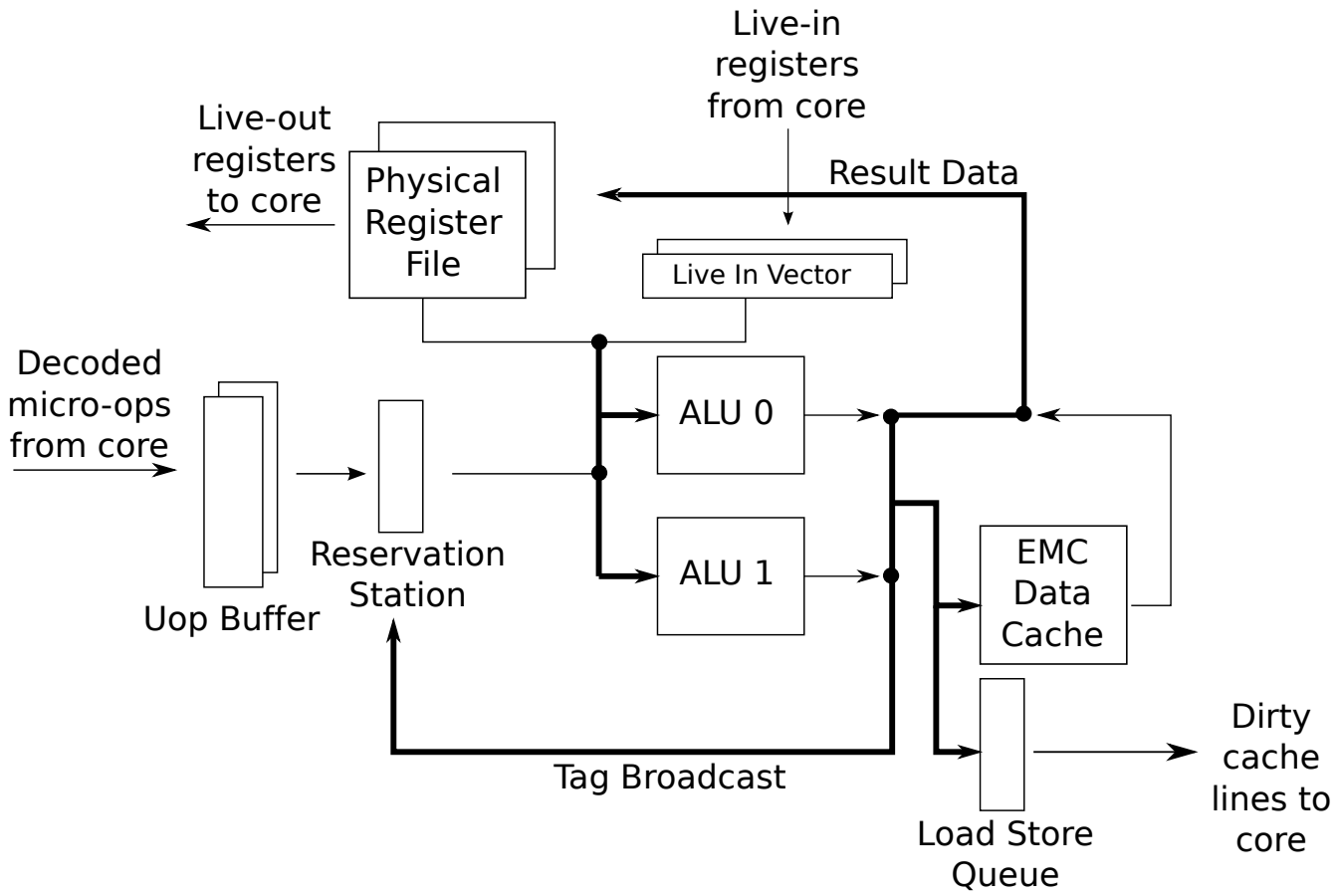
Dependent Cache Misses



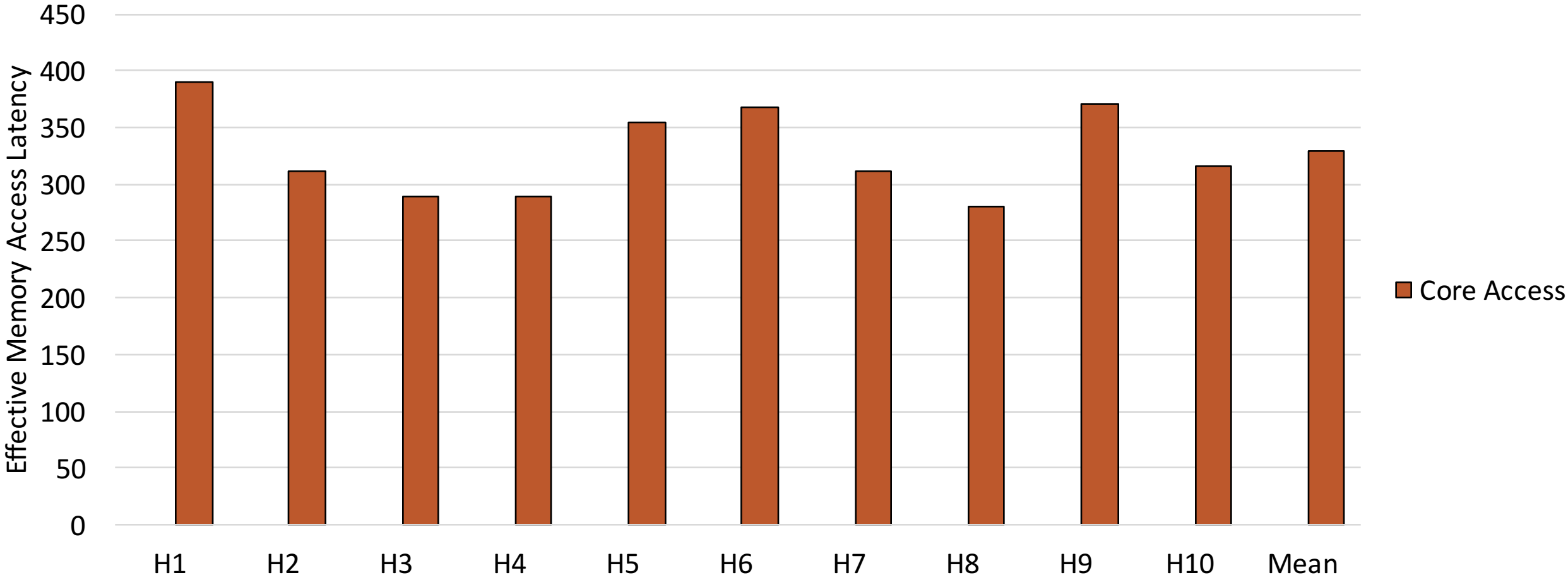
Dependent Cache Misses



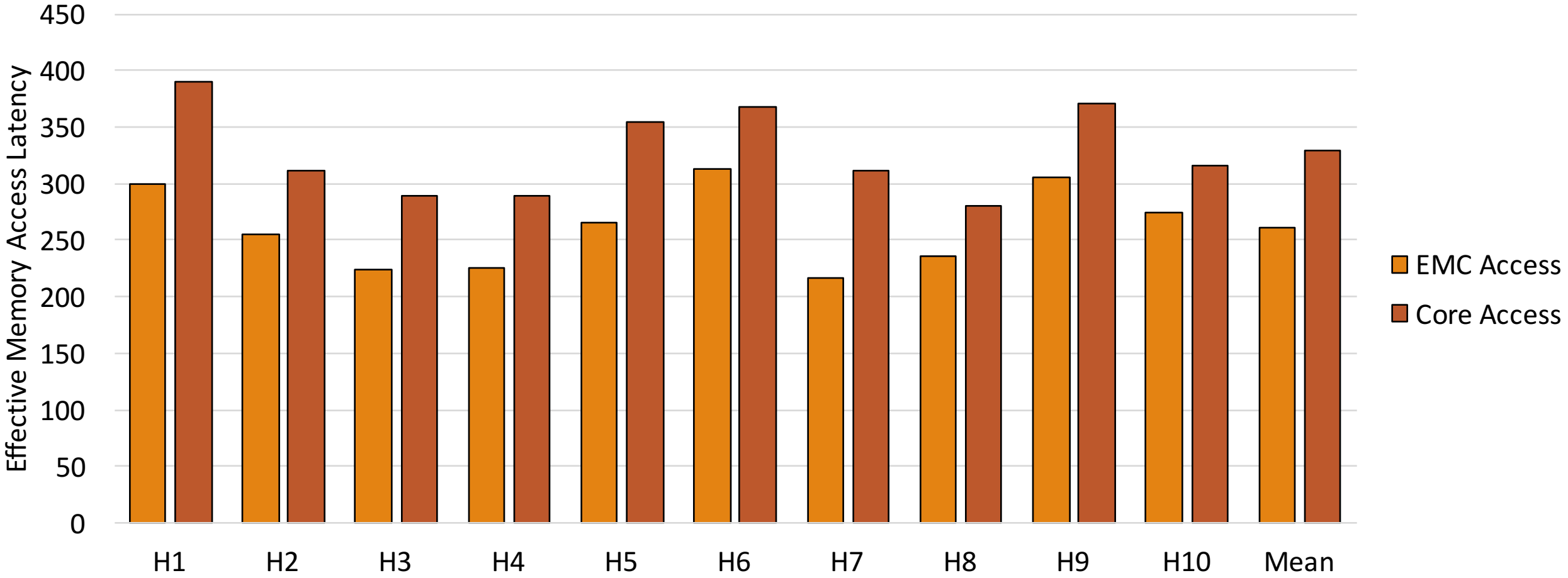
Compute Capable Memory Controller



Effective Memory Access Latency Reduction



Effective Memory Access Latency Reduction



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