Memory Compilers 5

Contents

OVERVIEW

This chapter contains information for memory compilers available in STDL80 cell library. These are complete compilers that consist of various generators to satisfy the requirements of the circuit at hand. Each of the final building block, the physical layout, will be implemented as a stand-alone, densely packed, pitch-matched array. Using this complex layout generator and adopting state-of-the-art logic and circuit design technique, these memory cells can realize extreme density and performance. In each layout generator, we added an option which makes the aspect ratio of the physical layout selectable so that the ASIC designers can choose the aspect ratio according to the convenience of the chip level layout.

In the STDL80 cell library, there are 4 groups of memory compilers — ROMs; Static RAMs; Register File; FIFO.

Generators

Each memory compiler is a set of various, parameterized generators. The generators are:

- Layout Generator
  : generates an array of custom, pitch-matched leaf cells.
- Schematic Generator & Netlister
  : extracts a netlist which can be used for both LVS check and functional verification.
- Function & Timing Model Generators
  : for gate level simulation, dynamic/static timing analysis and synthesis
- Symbol Generator
  : for schematic capture
- Critical Path Generator & ETC
  : there are many special purpose generators such as critical path generator used for both circuit design and AC timing characterization.

Advanced Design Technique

All of 0.5μm CMOS standard cell memory compilers adopt very advanced design technique to obtain extremely high performance in terms of both speed and power consumption. Below are major techniques.

For reducing power consumption

- Minimized bit-line precharge/discharge voltage swing
- Zero static current consuming sense amplifier
- Automatic power down after an access

For optimizing and minimizing the read access time

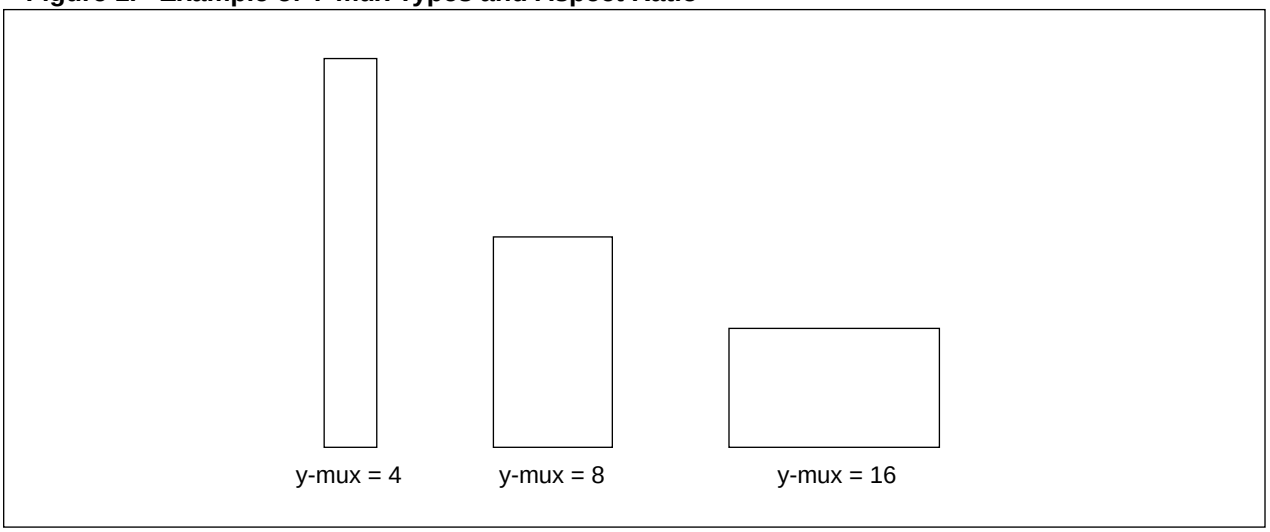
- Size sensitive self-timer delay
- Extremely simple tri-state output circuit

Flexible Aspect Ratio

The size of a memory cell is defined by its number of words (WORDS) and number of bits per word (BPW). But, this size is only a logical size. The physical size of a memory is defined by the number of rows (ROWS) and the number of columns (COLS) of its bit cell array. Usually, we can't make the bit cell array with WORDS and BPW because the range of WORDS is much larger than the range of BPW. If we make the bit cell array with WORDS and BPW, most of memory layouts will have too tall and too thin aspect ratio. Therefore, column decoder and y-mux circuit are included in most of memory cells to adjust the aspect ratio.

In 0.5μm CMOS standard cell memory compilers, the y-mux type selecting option was added to give the customers freedom selecting aspect ratio of the memory layout. Many of the characteristics of a memory cell are depend on its y-mux type. So, when you change the y-mux type from one to the other to change the aspect ratio, you have to know that it will change many major characteristics, such as access time, area and power consumption, of the memory.

< Figure 1. Example of Y-mux Types and Aspect Ratio >



Dual Banks

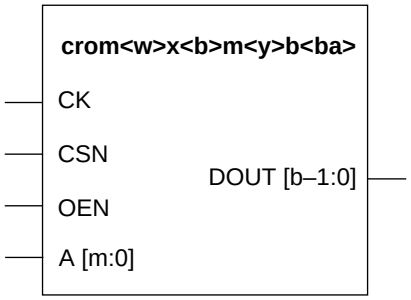
In some of 0.5μm CMOS standard cell memory compilers is a generator option which defines the number of bit array banks. This dual bank scheme doubles the maximum capacity of the memory compilers.

MEMORY COMPILERS SELECTION GUIDE

Memory Group	Cell Name	Function Description
ROM	CROM Gen	Contact Programmable Synchronous ROM Generator
	DROM Gen	Diffusion Programmable Synchronous ROM Generator
Static RAM	SPSRAM Gen	Single-Port Synchronous RAM Generator – Reads and writes at the same edge of clock
	SPSRAMA Gen	Single-Port Synchronous RAM Generator – Alternative – Reads and writes at different edges of clock
	SPARAM Gen	Single-Port Asynchronous RAM Generator – Fully asynchronous read, WEN synchronized write
	DPSRAM Gen	Dual-Port Synchronous RAM Generator – Reads and writes at the same edge of clock
	DPARAM* Gen	Dual-Port Asynchronous RAM Generator – Fully asynchronous read, WEN synchronized write
	DPSRAMA Gen	Dual-Port Synchronous RAM Generator – Alternative – Reads and writes at different edges of clock
Register File	IRIW*	1 Read Port, 1 Write Port Synchronous Register File
FIFO	FIFO*	Synchronous FIFO

* Under-Developed

Logic Symbol



NOTES:

1. Words (w) is the number of words in CROM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Static differential operation
- Stand-by (power down) mode available
- Tri-state output
- Low noise output circuit
- Programmable with contact layer
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 128K bits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

CROM Gen is a contact programmable synchronous ROM. When CK rises, DOUT [ ] presents data programmed in the location addressed by A [ ]. CSN is used to enable/disable the clock. OEN is used to enable/disable the data output driver.

Generators and Cell Configurations

CROM Gen. generates layout, netlist, symbol and functional & timing model of CROM. The layout of CROM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of CROM, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	32	64	128	256
		Max	1024	2048	4096	8192
		Step	8	16	32	64
Bpw (b)	ba = 1	Min	1	1	1	1
		Max	64	32	16	8
		Step	1	1	1	1
	ba = 2	Min	2	2	2	2
		Max	128	64	32	16
		Step	1	1	1	1

CROM Gen

Contact Programmable Synchronous ROM Generator

Pin Descriptions

Name	I/O	Description
CK	I	“Clock” serves as the input clock to the memory block. When CK is low the memory is in a precharge state. Upon the rising edge, an access cycle begins.
CSN	I	“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read access occur. CSN may not change during CK is high.
OEN	I	“Output Enable Negative” controls the output drivers from driven to tri-state condition. OEN may not change during CK is high.
A [ ]	I	“Address” selects the location to be accessed. A [ ] may not change during CK is high.
DOUT [ ]	O	During a read access, data word programmed will be presented to the “Data Out” ports. DOUT [ ] is tri-statable. When CK is high, CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state.

Pin Capacitance

(Unit = SL)

	CK	CSN	OEN	A	DOUT			
					Ymux 4	Ymux 8	Ymux 16	Ymux 32
1-bank	5.8	1.8	2.2	1.7	4.0	8.7	18.0	37.0
2-bank	11.5	3.7	4.4	1.7	4.0	8.7	18.0	37.0

Application Notes

1) Putting Busholders on DOUT [ ]

As you will see in the timing diagrams, DOUT [ ] is valid only when CK is high. If you want DOUT [ ] to be stable regardless of CK state, you should put STDL80 Busholder cells on the DOUT [ ] bus externally.

2) Customizing Aspect Ratio

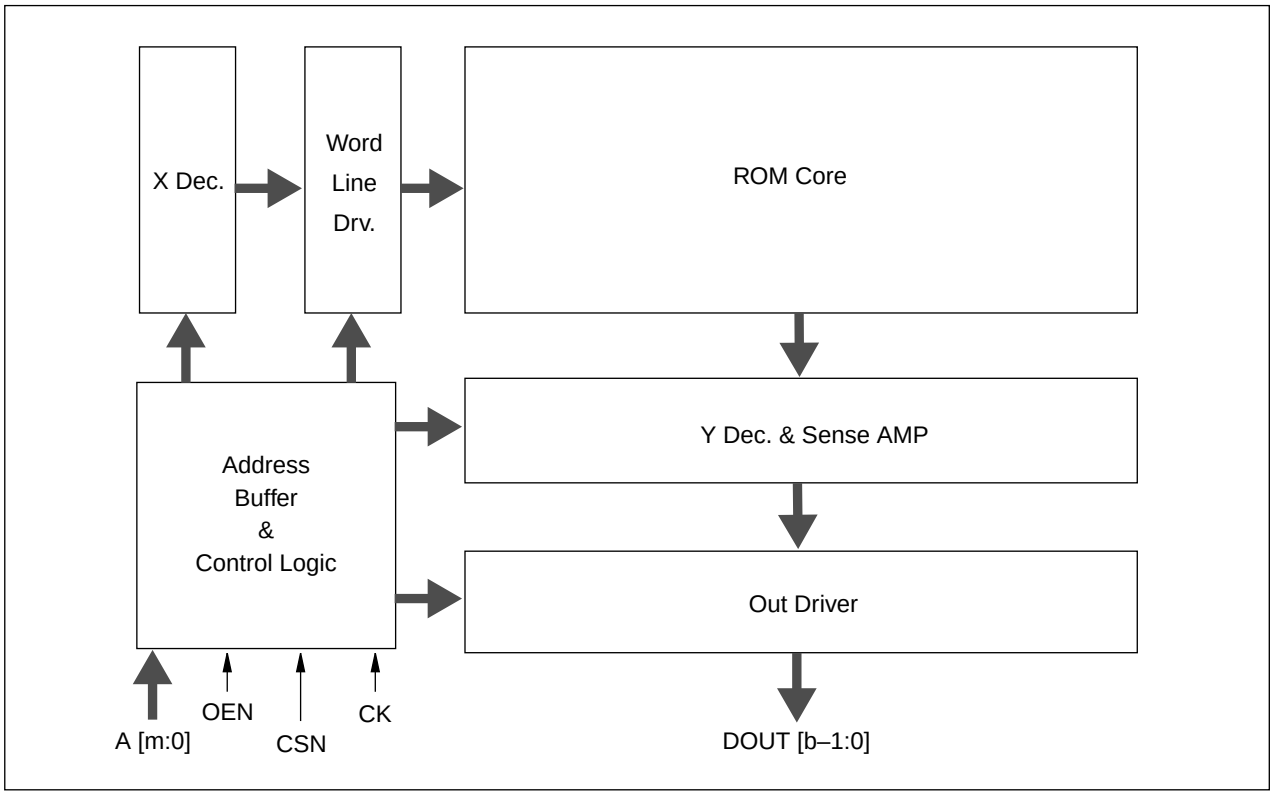
Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 4 selections of Ymux for the same Words and the same Bpw CROM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of CROM, In general, larger Ymux CROM has faster speed and bigger area than smaller Ymux CROM.

3) Selecting Number of Banks

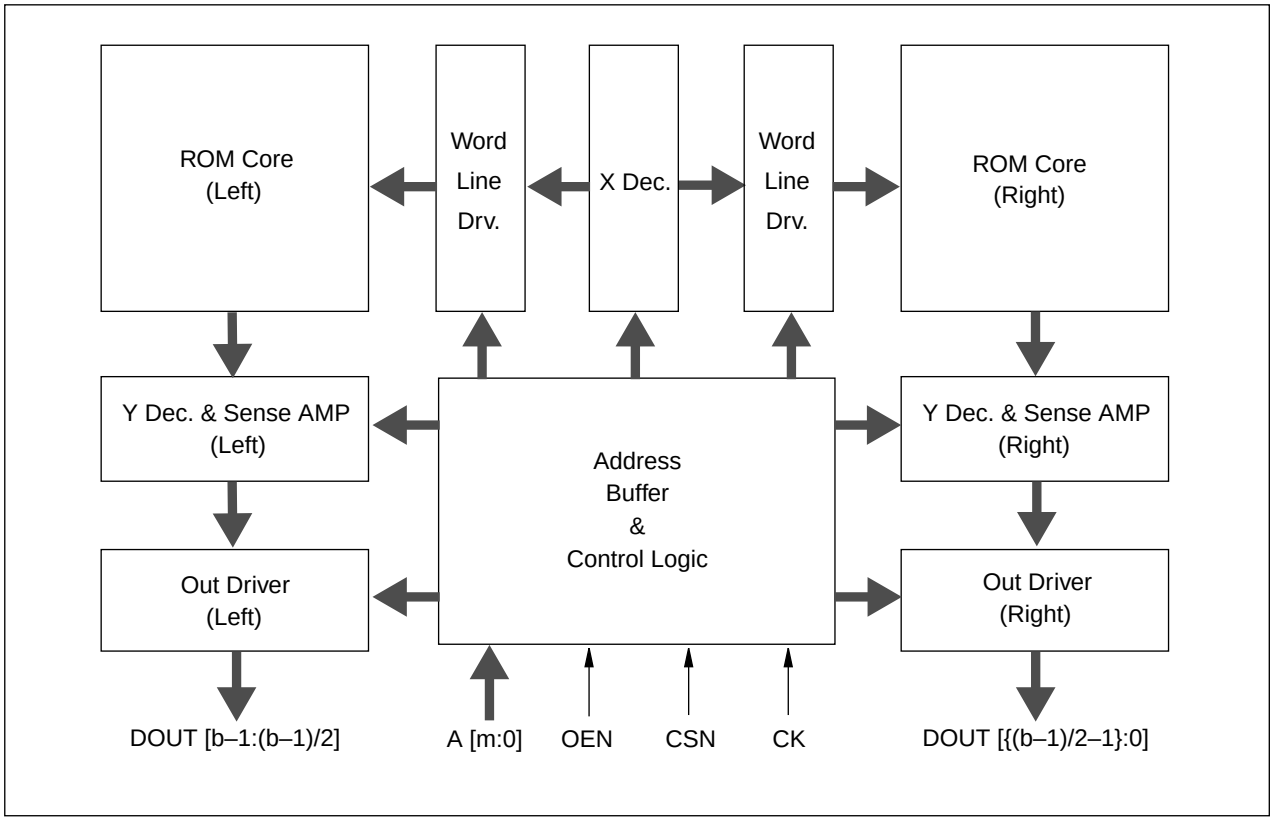
To enlarge the capacity of CROM, we added one more option to choose number of banks. If you want to use larger CROM than 64K bit CROM, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 64K bit CROM. Dual bank CROM is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

Block Diagrams

< 1-bank >



< 2-bank >



Characteristic Reference Table

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)							
minckl	Minimum Clock Pulse Width Low	2.80	2.80	3.20	3.20	4.20	4.20
minckh	Minimum Clock Pulse Width High	5.20	5.20	6.50	6.50	8.90	8.90
t_{as}	Address Setup Time	0.30	0.30	0.50	0.50	1.00	1.00
t_{ah}	Address Hold Time	0.30	0.30	1.40	1.40	1.80	1.80
t_{cs}	CSN Setup Time	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{os}	OEN Setup Time	0	0	0	0	0	0
t_{oh}	OEN Hold Time	1.90	1.80	2.00	1.90	2.10	2.00
t_{acc}	Access Time	3.20	3.20	3.60	3.60	4.40	4.40
t_{da}	Deaccess Time	2.00	2.00	2.00	2.00	2.00	2.00
SIZE (μm)							
Width		466	595	757	886	1329	1458
Height		443	443	638	638	1028	1028
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)			653		1426		3767
power_csn (stand-by mode: CSN High)			20		32		54

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
BA: Number of Banks (1 or 2)
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 4
minckh	(4.2863e – 03 * W + 1.6025e – 01 * S + 1.2091e – 01 * 0.02 * SL + 3.1188) * 1.1
minckl	(1.8303e – 03 * W + 2.4102e – 01 * S – 7.6923e – 03 * 0.02 * SL + 2.0153)
tacc	(1.5275e – 03 * W + 1.7051e – 01 * S + 3.4519e – 01 * 0.02 * SL + 2.4596)
	Y = 8
minckh	(2.1200e – 03 * W + 1.2948e – 01 * S + 1.2560e – 01 * 0.02 * SL + 3.1802) * 1.1
minckl	(9.1519e – 04 * W + 2.4102e – 01 * S – 7.6923e – 03 * 0.02 * SL + 2.0153)
tacc	(7.6375e – 04 * W + 1.7051e – 01 * S + 3.4519e – 01 * 0.02 * SL + 2.4596)
	Y = 16
minckh	(1.0472e – 03 * W + 1.6410e – 01 * S + 1.5997e – 01 * 0.02 * SL + 3.1662) * 1.1
minckl	(4.5759e – 04 * W + 2.4102e – 01 * S – 7.6923e – 03 * 0.02 * SL + 2.0153)
tacc	(3.8187e – 04 * W + 1.7051e – 01 * S + 3.4519e – 01 * 0.02 * SL + 2.4596)
	Y = 32
minckh	(5.0309e – 04 * W + 1.2435e – 01 * S + 2.4771e – 01 * 0.02 * SL + 3.2136) * 1.1
minckl	(2.2879e – 04 * W + 2.4102e – 01 * S – 7.6923e – 03 * 0.02 * SL + 2.0153)
tacc	(1.9093e – 04 * W + 1.7051e – 01 * S + 3.4519e – 01 * 0.02 * SL + 2.4596)

2) Power Characteristics [Unit: μW]

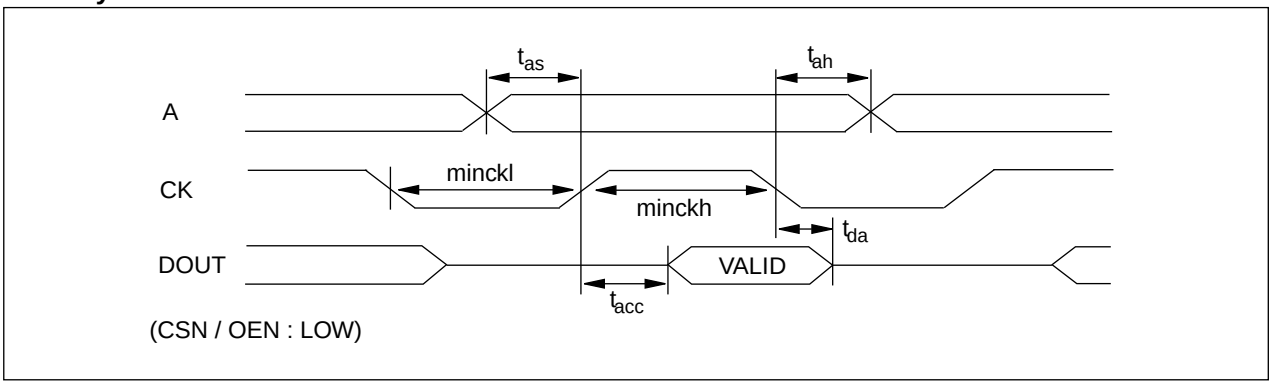
Power Type	Power Equation
	Y = 4
power_ck	(4.7057e – 02 * W + 1.7340 * B + 7.1595 + 3.2654e – 03 * W * B) * VDD^2 * F
power_csn	(–1.4914e – 05 * W + 6.7259e – 02 * B + 8.2631e – 01 + 1.1615e – 06 * W * B) * VDD^2 * F
	Y = 8
power_ck	(2.3345e – 02 * W + 2.9248 * B + 6.8769 + 3.2650e – 03 * W * B) * VDD^2 * F
power_csn	(–7.4573e – 06 * W + 1.3451e – 01 * B + 8.2631e – 01 + 1.1615e – 06 * W * B) * VDD^2 * F
	Y = 16
power_ck	(1.1254e – 02 * W + 5.2769 * B + 7.1131 + 3.1936e – 03 * W * B) * VDD^2 * F
power_csn	(–3.7287e – 06 * W + 2.6903e – 01 * B + 8.2631e – 01 + 1.1615e – 06 * W * B) * VDD^2 * F
	Y = 32
power_ck	(6.1194e – 03 * W + 1.0430e + 01 * B + 6.8749 + 2.9601e – 03 * W * B) * VDD^2 * F
power_csn	(–1.8643e – 06 * W + 5.3807e – 01 * B + 8.2631e – 01 + 1.1615e – 06 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

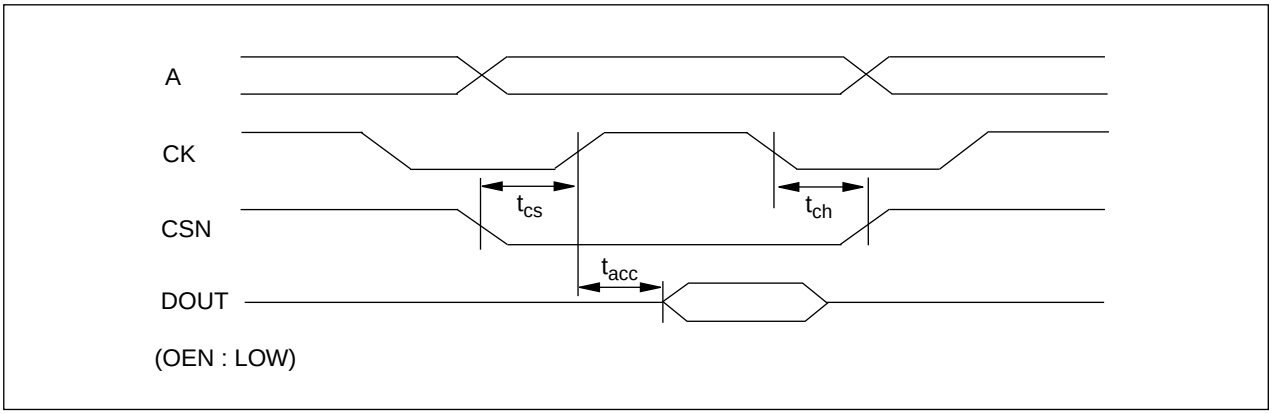
Width = 8.75 * (log2(W / Y)) + 129.65 * BA + 4.4 * (B * Y) + 1.4 [μm]
Height = 247.15 + 3.05 * W / Y [μm]

Timing Diagrams

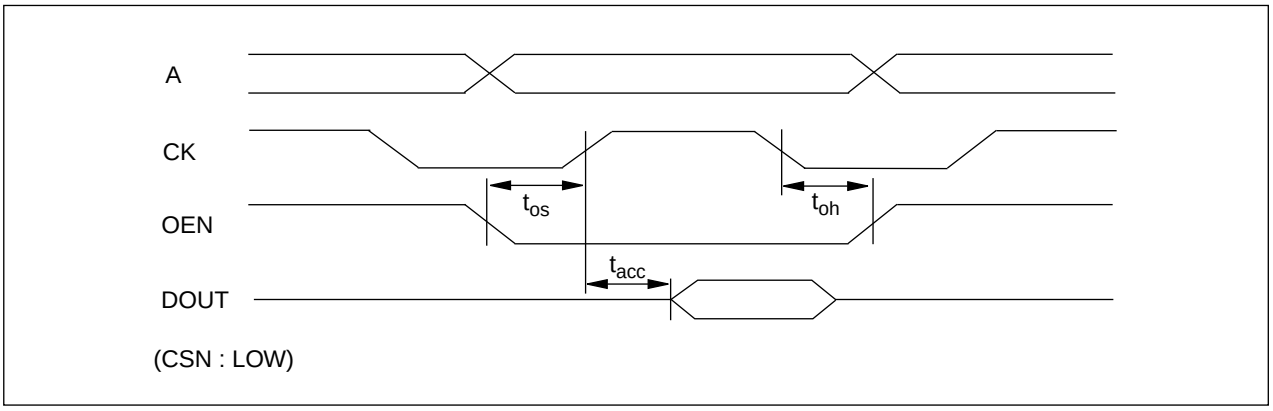
Read Cycle



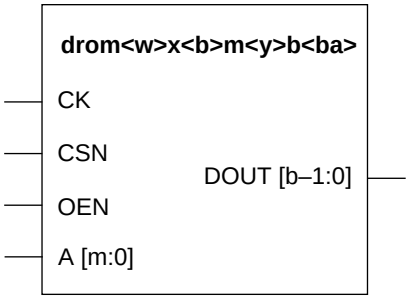
CSN Control



OEN Control



Logic Symbol



NOTES:

1. Words (w) is the number of words in a DROM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Stand-by (power down) mode available
- Latched output
- Unconditionally controlled tri-state output
- Low noise output circuit
- Programmable with diffusion layer
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 512K bits capacity
- Up to 16K number of words
- Up to 128 number of bits per word

Function Description

DROM is a diffusion programmable synchronous ROM. When CK rises, DOUT [ ] presents data programmed in the location addressed by A [ ]. CSN is used to enable/disable the clock. OEN is used to enable/disable the data output driver.

Generators and Cell Configurations

DROM Gen. generates layout, netlist, symbol and functional & timing model of DROM. The layout of DROM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of DROM, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	16	32	64
		Max	4096	8192	16384
		Step	16	32	64
Bpw (b)	ba = 1	Min	2	2	2
		Max	64	32	16
		Step	1	1	1
	ba = 2	Min	4	4	4
		Max	128	64	32
		Step	1	1	1

DROM Gen

Diffusion Programmable Synchronous ROM Generator

Pin Descriptions

Name	I/O	Description
CK	I	“Clock” serves as the input clock to the memory block. When CK is low the memory is in a precharge state. Upon the rising edge, an access cycle begins.
CSN	I	“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read access occur. CSN may not change during CK is high.
OEN	I	“Output Enable Negative” unconditionally controls the output drivers from driven to tri-state condition.
A [ ]	I	“Address” selects the location to be accessed. A [ ] may not change during CK is high.
DOUT [ ]	O	During a read access, data word programmed will be presented to the “Data Out” ports. DOUT [ ] is latched during a full cycle. When CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state.

Pin Capacitance

(Unit = SL)

	CK	CSN	OEN	A	DOUT
1-bank	2.1	0.6	1.1	2.3	44.0
2-bank	4.2	1.2	2.2	2.3	44.0

Application Notes

1) Customizing Aspect Ratio

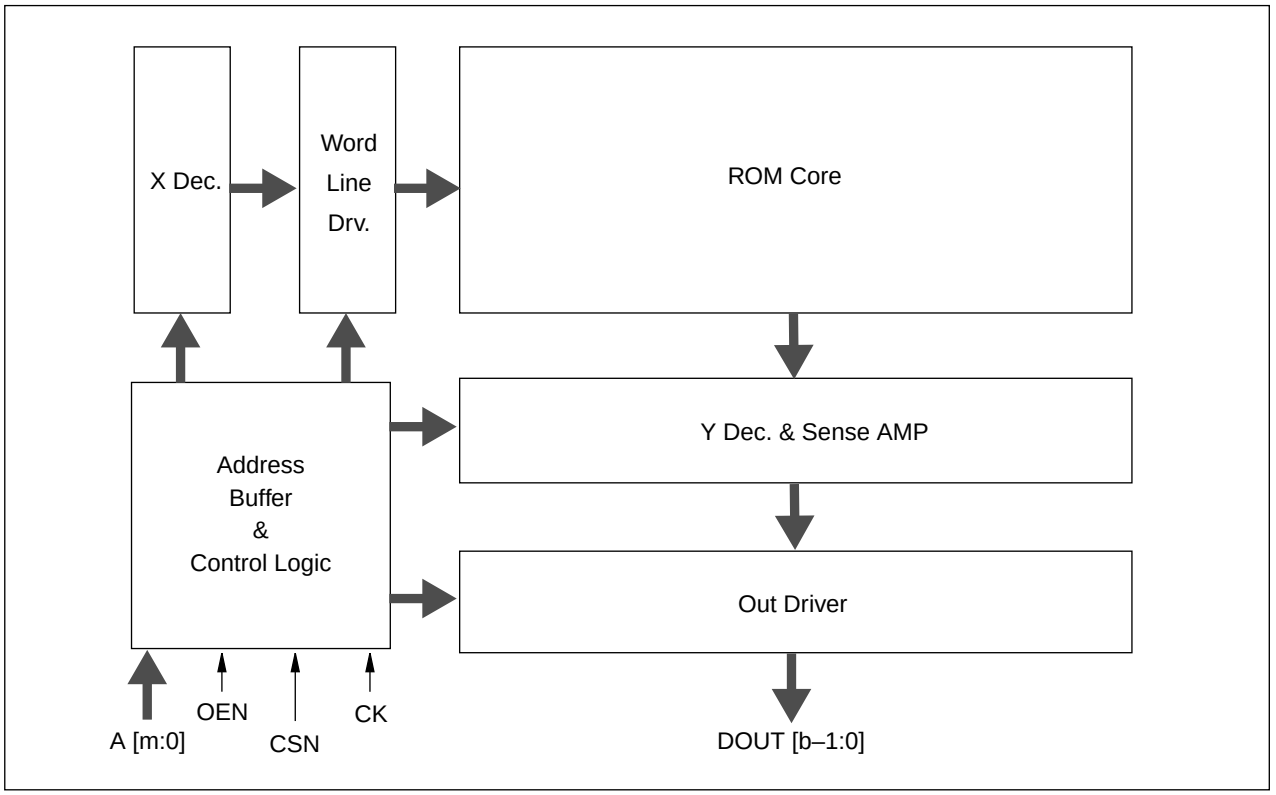
Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 3 selections of Ymux for the same Words and the same Bpw DROM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of DROM, In general, larger Ymux DROM has faster speed and bigger area than smaller Ymux DROM.

2) Selecting Number of Banks

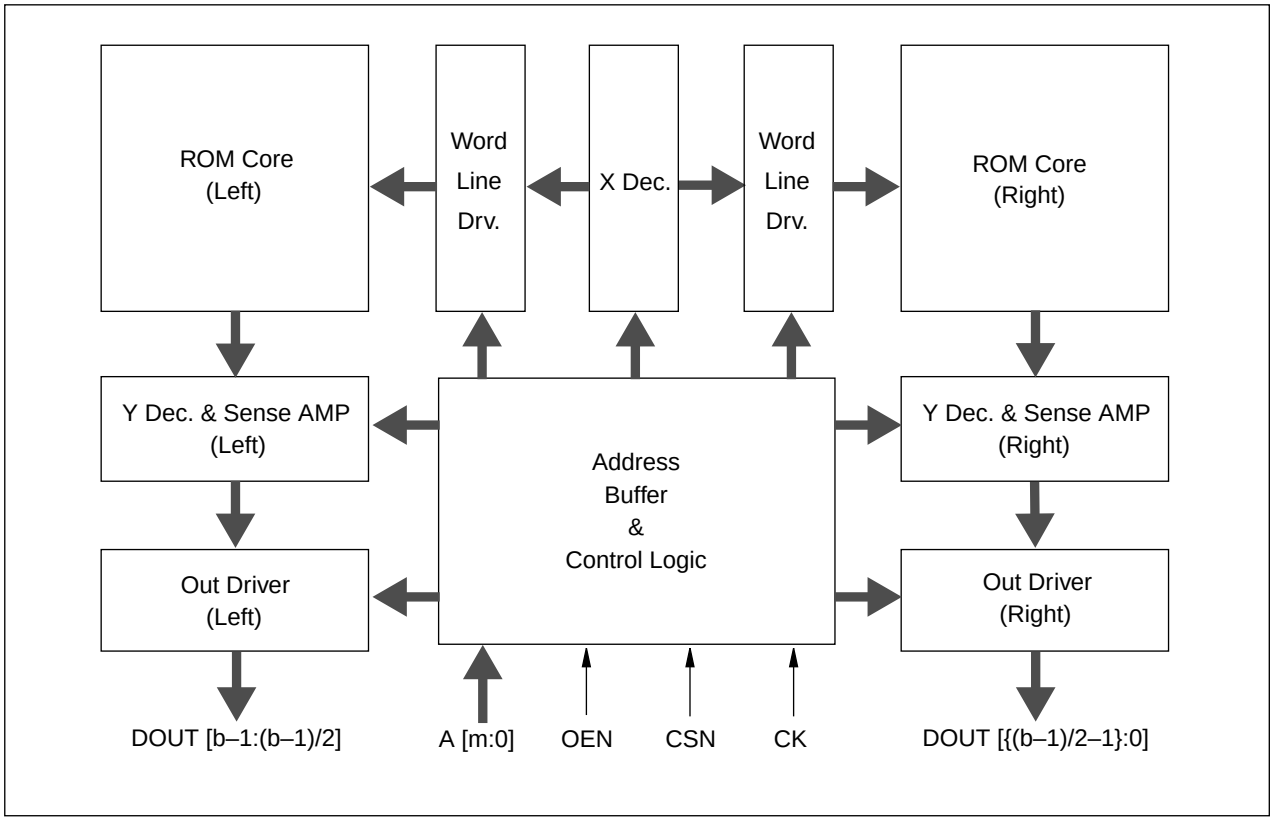
To enlarge the capacity of DROM, we added one more option to choose number of banks. If you want to use larger DROM than 256K bit DROM, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 256K bit DROM. Dual bank DROM is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

Block Diagrams

< 1-bank >



< 2-bank >



DROM Gen

Diffusion Programmable Synchronous ROM Generator

Characteristic Reference Table

Symbol	Description	256x16m8		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)							
minckl	Minimum Clock Pulse Width Low	1.80	1.70	1.80	1.70	2.10	1.80
minckh	Minimum Clock Pulse Width High	4.70	4.50	5.40	5.20	6.90	6.50
t_{as}	Address Setup Time	0.28	0.28	0.31	0.31	0.32	0.32
t_{ah}	Address Hold Time	0	0	0	0	0	0
t_{cs}	CSN Setup Time	0.44	0.44	0.44	0.44	0.44	0.44
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{acc}	Access Time	5.60	5.40	6.20	6.00	7.50	7.10
t_{da}	Deaccess Time	4.10	4.00	4.80	4.60	6.0	5.60
t_{zd}	Hi-Z to Valid Data	1.90	1.90	1.90	1.90	1.90	1.90
t_{dz}	Valid Data to Hi-Z	1.60	1.50	1.60	1.50	1.70	1.60
mincyc	Minimum Clock Cycle Time	6.10	5.80	8.00	7.80	11.30	10.80
SIZE (μm)							
Width		556	720	576	740	917	1081
Height		305	305	526	526	823	823
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)			390		749		2027
power_csn (stand-by mode: CSN High)			9.8		9.8		16

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
BA: Number of Banks (1 or 2)
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 8
mincyc	(2.5468e – 03 * W + 3.1940e – 02 * B / BA + 1.0384e – 01 * S + 4.7966)
minckh	(8.4451e – 04 * W + 2.3114e – 02 * B / BA + 7.1153e – 02 * S + 4.0270)
minckl	(1.3917e – 02 * B / BA + 2.8361e – 01 * S + 1.2142 + 1.5719e – 03 * B / BA * S)
tacc	(8.4234e – 04 * W + 2.3033e – 02 * B / BA + 1.0288e – 01 * S + 5.8079e – 01 * 0.02 * SL + 4.7546)
	Y = 16
mincyc	(1.2326e – 03 * W + 6.7538e – 02 * B / BA + 2.7115e – 01 * S +4.8548)
minckh	(4.2208e – 04 * W + 4.6630e – 02 * B / BA + 8.6538e – 02 * S + 4.3200)
minckl	(2.7834e – 02 * B / BA + 2.8361e – 01 * S + 1.2142 + 3.1438e – 03 * B / BA * S)
tacc	(4.2117e – 04 * W + 4.6066e – 02 * B / BA + 1.0288e – 01 * S + 5.8079e – 01 * 0.02 * SL + 4.7546)
	Y = 32
mincyc	(5.8723e – 04 * W + 1.4387e – 01 * B / BA + 1.8942e – 01 * S + 5.4184)
minckh	(2.1195e – 04 * W + 9.2951e – 02 * B / BA + 9.7115e – 02 * S + 4.9479)
minckl	(5.5668e – 02 * B / BA + 2.8361e – 01 * S + 1.2142 + 6.2876e – 03 * B / BA * S)
tacc	(2.1058e – 04 * W + 9.2132e – 02 * B / BA + 1.0288e – 01 * S + 5.8079e – 01 * 0.02 * SL + 4.7546)

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 8
power_ck	(1.7976e – 02 * W + 1.2560 * B + 5.7252 + 1.4992e – 03 * W * B) * VDD^2 * F
power_csn	(–1.8602e – 05 * W + 3.0168e – 02 * B + 4.1766e – 01 + 1.9173e – 06 * W * B) * VDD^2 * F
	Y = 16
power_ck	(8.6750e – 03 * W + 2.0183 * B + 5.6958 + 1.7184e – 03 * W * B) * VDD^2 * F
power_csn	(–9.3013e – 06 * W + 6.0336e – 02 * B + 4.1766e – 01 + 1.9173e – 06 * W * B) * VDD^2 * F
	Y = 32
power_ck	(4.1580e – 03 * W + 4.1059 * B + 6.0523 + 1.8497e – 03 * W * B) * VDD^2 * F
power_csn	(–4.6506e – 06 * W + 1.2067e – 01 * B + 4.1766e – 01 + 1.9173e – 06 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

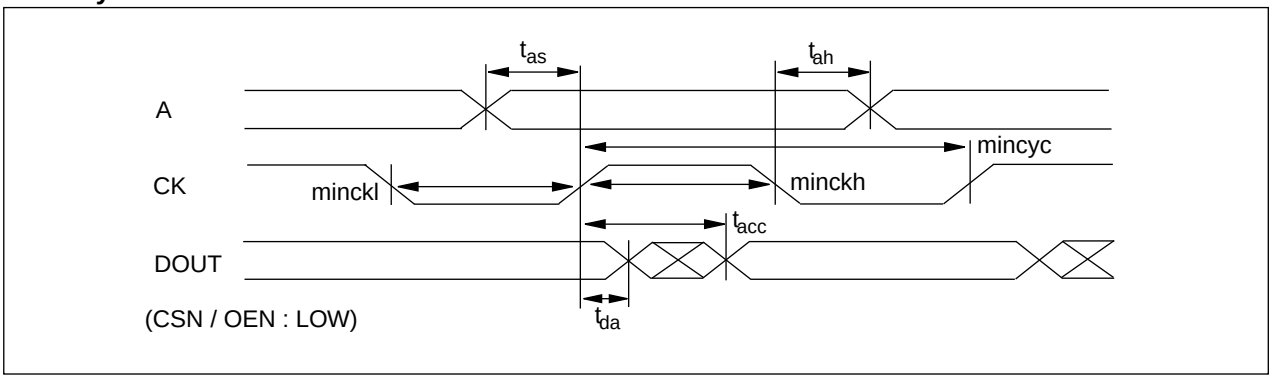
Width = 10.2 * ($\lceil \log_2 (W / Y) \rceil$) + 164.8 * BA + 2.5843(B * Y) + 8.2 [μm]

Height = 225.1 + 2.30 * W / Y + M [μm]

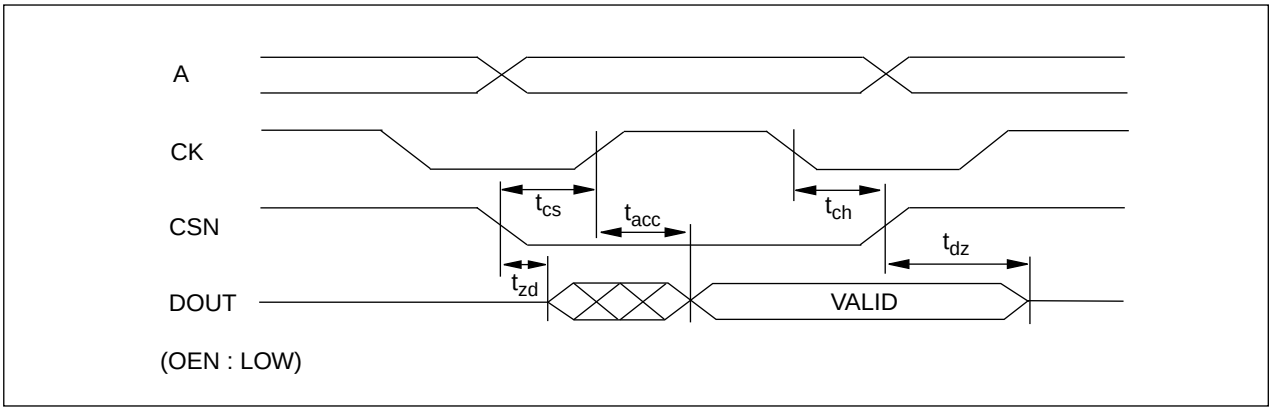
M = 6.05 (if Y = 8), M = 8.45 (if Y = 16), M = 10.85 (if Y = 32)

Timing Diagrams

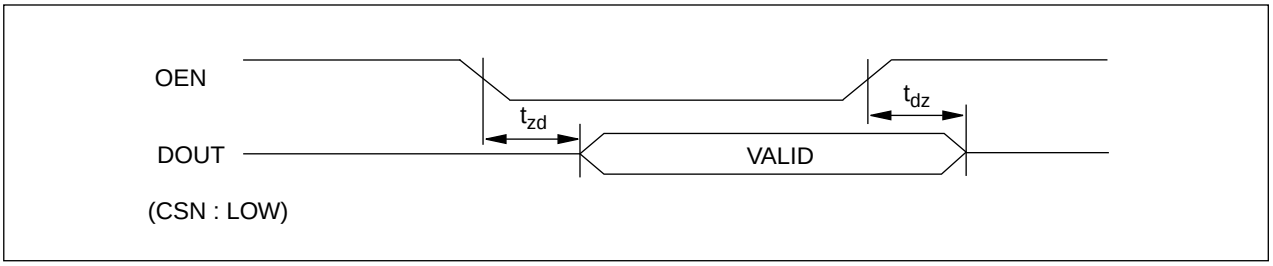
Read Cycle



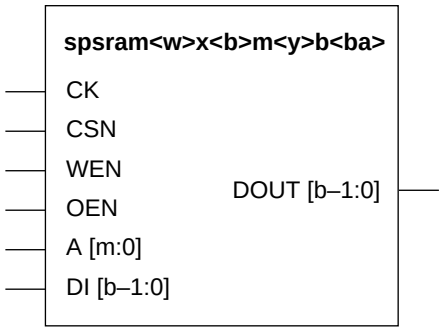
CSN Control



OEN Control



Logic Symbol



NOTES:

1. Words (w) is the number of words in SPSRAM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Write completed at rising edge of clock
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 128K bits capacity
- Up to 8K number of words
- Up to 256 number of bits per word

Function Description

SPSRAM is a single-port synchronous static RAM. When CK rises, if WEN is high, DOUT [ ] presents data stored in the location addressed by A [ ], otherwise the value of DI [ ] is written into the location addressed by A [ ]. CSN is used to enable/disable the clock. OEN is used to enable/disable the data output driver.

Generators and Cell Configurations

SPSRAM Gen. generates layout, netlist, symbol and functional & timing model of SPSRAM. The layout of SPSRAM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of SPSRAM, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	4	8	16	32	64
		Max	512	1024	2048	4096	8192
		Step	2	4	8	16	32
Bpw (b)	ba = 1	Min	1	1	1	1	1
		Max	128	64	32	16	8
		Step	1	1	1	1	1
	ba = 2	Min	2	2	2	2	2
		Max	256	128	64	32	16
		Step	1	1	1	1	1

SPSRAM Gen

Single-Port Synchronous RAM Generator

Pin Descriptions

Name	I/O	Input Cap.	Description
CK	I		“Clock” serves as the input clock to the memory block. When CK is low, the memory is in a precharge state. Upon the rising edge, an access begins.
CSN	I		“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read or write access occur. CSN may not change during CK is high.
WEN	I		“Write Enable Negative” selects the type of memory access. Read is the high state, and write is the low state.
OEN	I		“Output Enable Negative” controls the output drivers from driven to tri-state condition. OEN may not change during CK is high.
A [ ]	I		“Address” selects the location to be accessed. A [ ] may not change during CK is high.
DI [ ]	I		When CK rises while WEN is low, the “Data In” word value is written to the accessed location.
DOUT [ ]	O		During a read access, data word stored will be presented to the “Data Out” ports. DOUT [ ] is tri-statable. When CK is high, CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state. During a write access, data word written will be presented at the “Data Out” ports if output driver is enabled.

Pin Capacitance

(Unit = SL)

	CK	CSN	WEN	OEN	A	DI	DOUT				
							Ymux 2	Ymux 4	Ymux 8	Ymux 16	Ymux 32
1-bank	3.5	1.0	0.5	1.6	1.2	2.1	3.1	3.3	7.7	15.0	31.0
2-bank	7.0	2.1	1.0	3.1	1.2	2.1	3.1	3.3	7.7	15.0	31.0

Application Notes

1) Putting Busholders on DOUT [ ]

As you will see in the timing diagrams, DOUT [ ] is valid only when CK is high. If you want DOUT [ ] to be stable regardless of CK state, you should put STDL80 Busholder cells on the DOUT [ ] bus externally.

2) Customizing Aspect Ratio

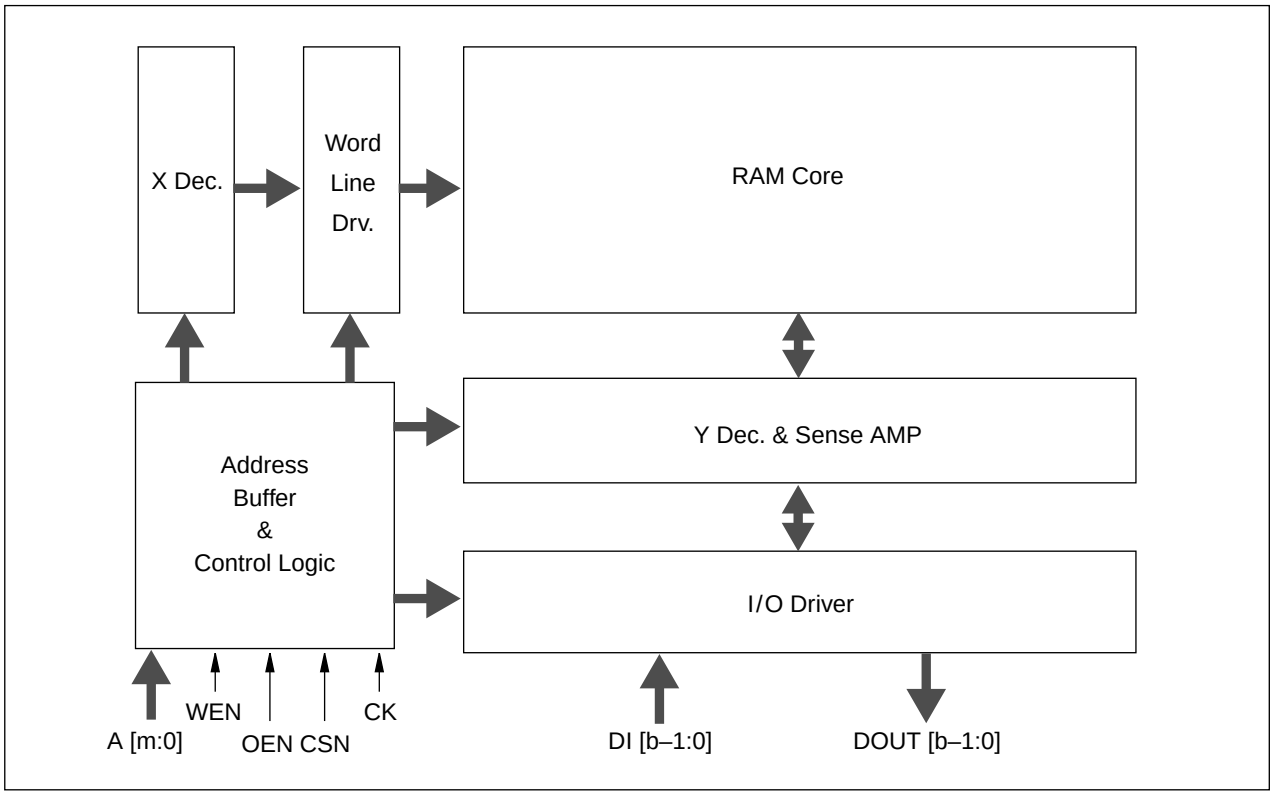
Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 5 selections of Ymux for the same Words and the same Bpw SPSRAM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of SPSRAM, In general, larger Ymux SPSRAM has faster speed and bigger area than smaller Ymux SPSRAM.

3) Selecting Number of Banks

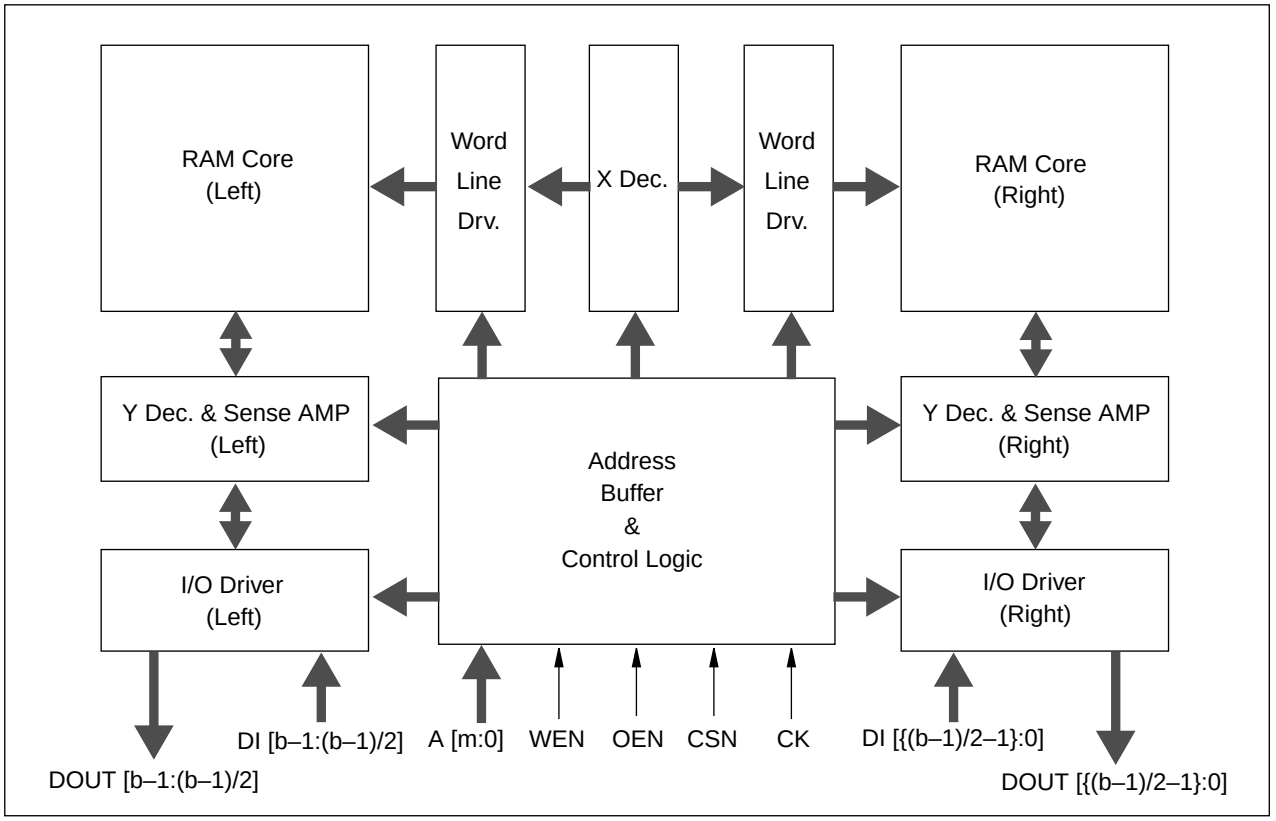
To enlarge the capacity of SPSRAM, we added one more option to choose number of banks. If you want to use larger SPSRAM than 64K bit SPSRAM, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 64K bit SPSRAM. Dual bank SPSRAM is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

Block Diagrams

< 1-bank >



< 2-bank >



Characteristic Reference Table

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)							
minckl	Minimum Clock Pulse Width Low	2.10	2.00	2.50	2.40	3.30	3.10
minckh	Minimum Clock Pulse Width High	5.90	5.90	6.30	6.20	6.90	6.70
t_{as}	Address Setup Time	0.30	0.30	0.50	0.50	0.70	0.70
t_{ah}	Address Hold Time	6.30	6.30	0.40	0.40	0.40	0.40
t_{cs}	CSN Setup Time	0.40	0.40	0.40	0.40	0.40	0.40
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{ds}	Data Input Setup Time	0	0	0	0	0	0
t_{dh}	Data Input Hold Time	3.00	2.80	3.70	3.40	5.10	4.70
t_{os}	OEN Setup Time	0	0	0	0	0	0
t_{oh}	OEN Hold Time	1.70	1.70	1.90	1.80	2.20	2.00
t_{ws}	WEN Setup Time	0	0	0	0	0	0
t_{wh}	WEN Hold Time	0	0	0	0	0	0
t_{acc}	Access Time	3.20	3.10	3.70	3.50	4.90	4.50
t_{da}	Deaccess Time	2.30	2.20	2.50	2.30	2.70	2.30
mincyc	Minimum Clock Cycle Time	8.20	8. 0	9.40	9.00	11.80	11.00
SIZE (μm)							
Width		622	703	1131	1212	2142	2222
Height		902	902	1501	1501	2697	2697
POWER (μW/MHz)							
power_ck (normal mode: CSN Low)			593		1165		2403
power_csn (stand-by mode: CSN High)			54		96		155

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
B: Bits per Word
Y: Ymux Type
BA: Number of Banks (1 or 2)
S: Input Slope (Unit: ns)
SL: Number of Fanouts (Unit: Standard Load)
VDD: Operating Voltage (Unit: V)
F: Operating Frequency (Unit: MHz)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
cycle_time	(5.8213e – 03 * W + 1.1171e – 02 * B / BA + 9.6628e – 01 * 0.02 * SL + 3.7318) * 1.08
minckh	(1.9096e – 03 * W + 2.4791e – 03 * B / BA + 1.2200 * 0.02 * SL + 2.1295)
minckl	(2.1603e – 03 * W + 3.5437e – 03 * B / BA + 1.7035 + 2.8208e – 07 * W * B / BA)
tacc	(2.8038e – 03 * W + 5.8650e – 03 * B / BA + 1.7115e – 01 * S + 4.9717e – 01 * 0.02 * SL + 2.3023)
	Y = 4
cycle_time	(2.9106e – 03 * W + 2.2342e – 02 * B / BA + 9.6628e – 01 * 0.02 * SL + 3.7318) * 1.08
minckh	(9.5482e – 04 * W + 4.9583e – 03 * B / BA + 1.2200 * 0.02 * SL + 2.1295)
minckl	(1.0801e – 03 * W + 7.0874e – 03 * B / BA + 1.7035 + 2.8207e – 07 * W * B / BA)
tacc	(1.4019e – 03 * W + 1.1730e – 02 * B / BA + 1.7115e – 01 * S + 4.9717e – 01 * 0.02 * SL + 2.3023)
	Y = 8
cycle_time	(1.4553e – 03 * W + 4.4684e – 02 * B / BA + 9.6628e – 01 * 0.02 * SL + 3.7318) * 1.08
minckh	(4.7741e – 04 * W + 9.9166e – 03 * B / BA + 1.2200 * 0.02 * SL + 2.1295)
minckl	(5.4009e – 04 * W + 1.4174e – 02 * B / BA + 1.7035 + 2.8208e – 07 * W * B / BA)
tacc	(7.0097e – 04 * W + 2.3460e – 02 * B / BA + 1.7115e – 01 * S + 4.9717e – 01 * 0.02 * SL + 2.3023)
	Y = 16
cycle_time	(7.2766e – 04 * W + 8.9369e – 02 * B / BA + 9.6628e – 01 * 0.02 * SL + 3.7318) * 1.08
minckh	(2.3870e – 04 * W + 1.9833e – 02 * B / BA + 1.2200 * 0.02 * SL + 2.1295)
minckl	(2.7004e – 04 * W + 2.8349e – 02 * B / BA + 1.7035 + 2.8208e – 07 * W * B / BA)
tacc	(3.5048e – 04 * W + 4.6920e – 02 * B / BA + 1.7115e – 01 * S + 4.9717e – 01 * 0.02 * SL + 2.3023)
	Y = 32
cycle_time	(3.6383e – 04 * W + 1.7873e – 01 * B / BA + 9.6628e – 01 * 0.02 * SL + 3.7318) * 1.08
minckh	(1.1935e – 04 * W + 3.9666e – 02 * B / BA + 1.2200 * 0.02 * SL + 2.1295)
minckl	(1.3502e – 04 * W + 5.6699e – 02 * B / BA + 1.7035 + 2.8205e – 07 * W * B / BA)
tacc	(1.7524e – 04 * W + 9.3840e – 02 * B / BA + 1.7115e – 01 * S + 4.9717e – 01 * 0.02 * SL + 2.3023)

2) Power Characteristics [Unit: μW]

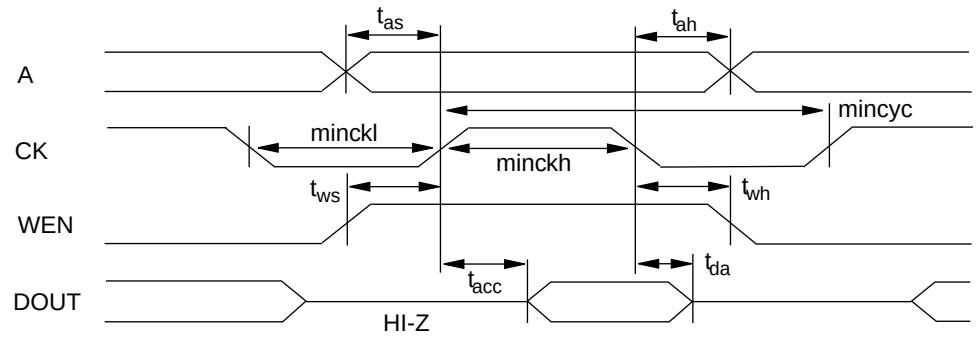
Power Type	Power Equation
	Y = 2
power_ck	(1.7046e – 01 * W + 8.7926e – 01 * B + 1.2869 + 7.9009e – 04 * W * B) * VDD^2 * F
power_csn	(4.6346e – 03 * W + 1.3484e – 01 * B + 5.8215e – 01 – 9.0563e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(8.5232e – 02 * W + 1.7585 * B + 1.2869 + 7.9009e – 04 * W * B) * VDD^2 * F
power_csn	(2.3173e – 03 * W + 2.6969e – 01 * B + 5.8215e – 01 – 9.0563e – 05 * W * B) * VDD^2 * F
	Y = 8
power_ck	(4.1803e – 02 * W + 3.3360 * B + 3.3968e – 01 + 6.4193e – 04 * W * B) * VDD^2 * F
power_csn	(1.1586e – 03 * W + 5.3939e – 01 * B + 5.8215e – 01 – 9.0563e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(1.8749e – 02 * W + 5.2054 * B + 3.5471 + 8.7095e – 04 * W * B) * VDD^2 * F
power_csn	(5.7933e – 04 * W + 1.0787 * B + 5.8215e – 01 – 9.0563e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(9.0824e – 03 * W + 9.4829 * B + 4.6843 + 7.9026e – 04 * W * B) * VDD^2 * F
power_csn	(2.8966e – 04 * W + 2.1575 * B + 5.8215e – 01 – 9.0563e – 05 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 6 * ($\lceil \log_2 (W / Y) \rceil$) + 76.3 * BA + 4.4(B * Y / 4 + BA) + 6.75 * B * Y + 2.25 [μm]
Height = 297.5 + 9.35 * W / Y + M [μm]
M = 5.75 (if Y = 2, 4, 8, 16), M = 8.15 (if Y = 32)

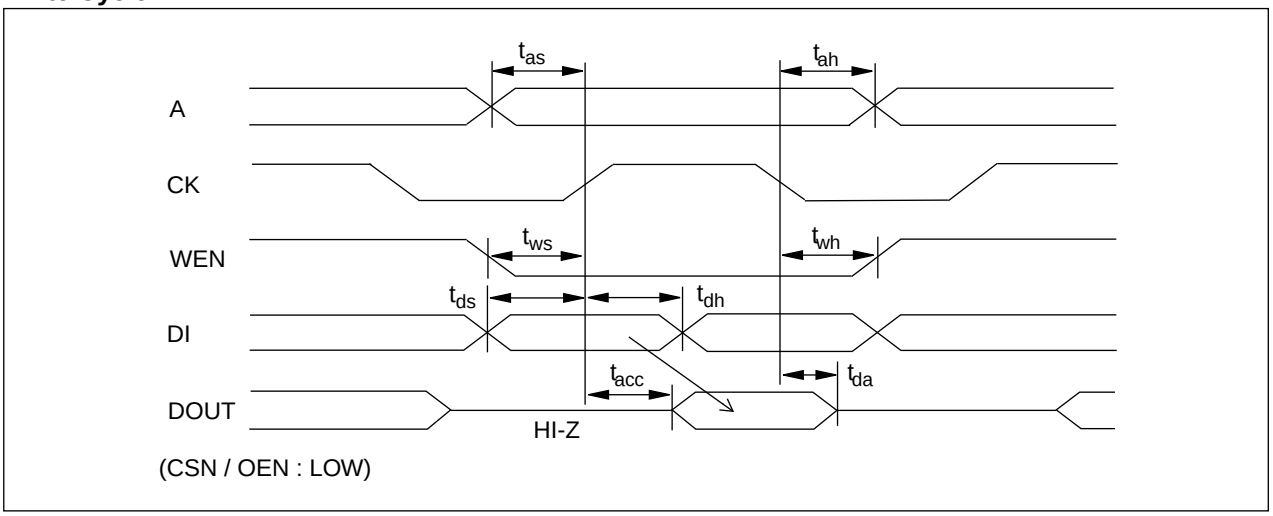
Timing Diagrams

Read Cycle

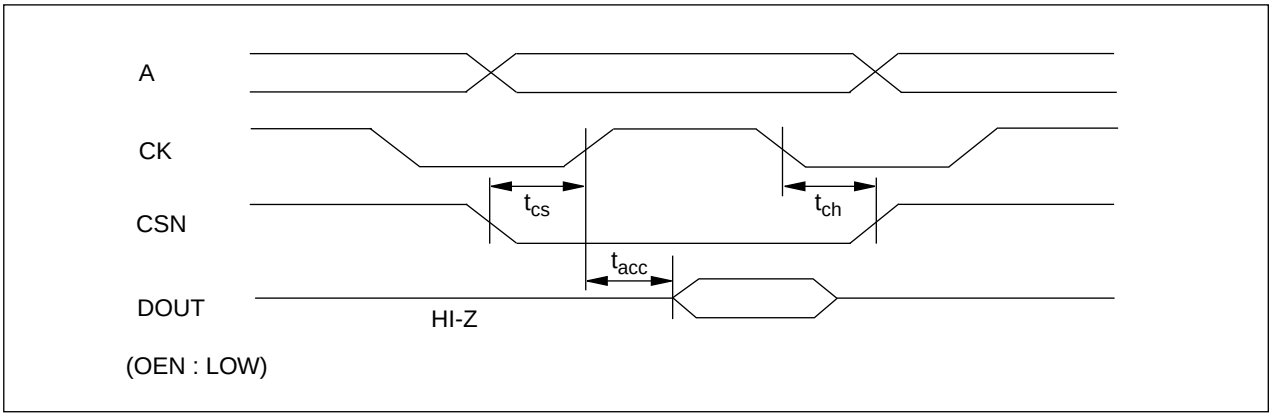


(CSN / OEN : LOW)

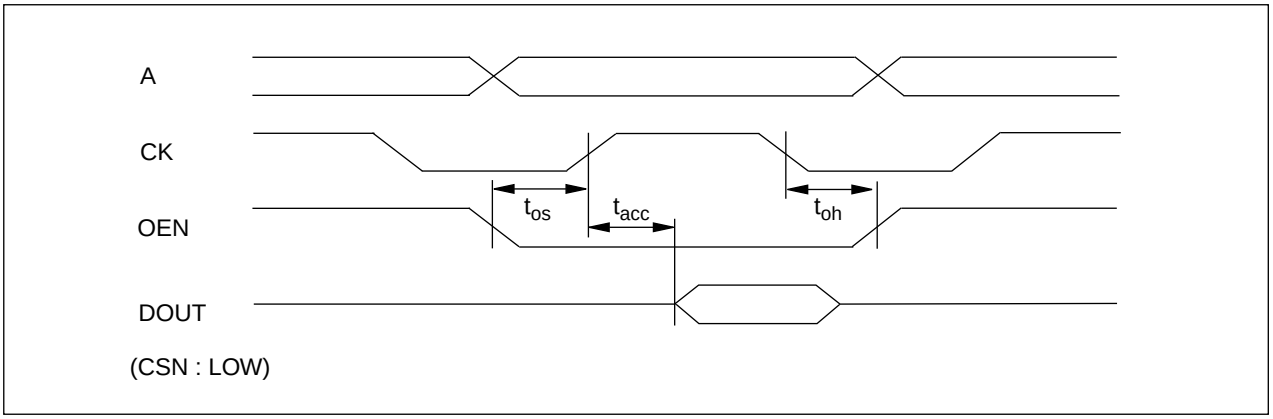
Write Cycle



CSN Control



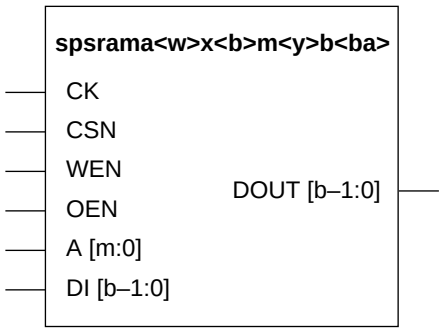
OEN Control



SPSRAMA Gen

Single-Port Synchronous RAM Generator – Alternative

Logic Symbol



NOTES:

1. Words (w) is the number of words in SPSRAMA.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Write completed at falling edge of clock
- Possible read modified write cycle
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Possible bi-directional operation
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 128K bits capacity
- Up to 8K number of words
- Up to 256 number of bits per word

Function Description

SPSRAMA is a single-port synchronous static RAM. When WEN is high and CK rises, DOUT [ ] presents data stored in the location addressed by A [ ]. When WEN is low and CK falls, or when CK is high and WEN rises, the value of DI [ ] is written into the location addressed by A [ ]. CSN is used to enable/disable the clock. OEN is used to enable/disable the data output driver.
SPSRAMA is an alternative of SPSRAM. The major difference of these two RAMs is the timing of read and write. SPSRAMA reads and writes at different edge of the clock since SPSRAM reads and writes at the same edge of the clock.

Generators and Cell Configurations

SPSRAMA Gen. generates layout, netlist, symbol and functional & timing model of SPSRAMA. The layout of SPSRAMA is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of SPSRAMA, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	4	8	16	32	64
		Max	512	1024	2048	4096	8192
		Step	2	4	8	16	32
Bpw (b)	ba = 1	Min	1	1	1	1	1
		Max	128	64	32	16	8
		Step	1	1	1	1	1
	ba = 2	Min	2	2	2	2	2
		Max	256	128	64	32	16
		Step	1	1	1	1	1

Pin Descriptions

Name	I/O	Description
CK	I	“Clock” serves as the input clock to the memory block. When CK is low, the memory is in a precharge state. Upon the rising edge, a read cycle begins. Upon the falling edge, a write cycle ends.
CSN	I	“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read or write access occur. CSN may not change during CK is high.
WEN	I	“Write Enable Negative” selects the type of memory access. Read is the high state, and write is the low state. When WEN rises while CK is high, a write cycle ends.
OEN	I	“Output Enable Negative” controls the output drivers from driven to tri-state condition. OEN may not change during CK is high.
A [ ]	I	“Address” selects the location to be accessed. A [ ] may not change during CK is high.
DI [ ]	I	When CK falls while WEN is low, or when WEN rises while CK is high, the “Data In” word value is written to the accessed location.
DOUT [ ]	O	During a read access, data word stored will be presented to the “Data Out” ports. DOUT [ ] is tri-statable. When CK is high, CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state. During a write access, the value of DOUT [ ] is unpredictable.

Pin Capacitance

(Unit = SL)

	CK	CSN	WEN	OEN	A	DI	DOUT				
							Ymux 2	Ymux 4	Ymux 8	Ymux 16	Ymux 32
1-bank	3.5	1.0	0.5	1.6	1.2	2.1	3.1	3.3	7.7	15.0	31.0
2-bank	7.0	2.1	1.0	3.1	1.2	2.1	3.1	3.3	7.7	15.0	31.0

Application Notes

1) Putting Busholders on DOUT [ ]

As you will see in the timing diagrams, DOUT [ ] is valid only when CK is high. If you want DOUT [ ] to be stable regardless of CK state, you should put STDL80 Busholder cells on the DOUT [ ] bus externally.

2) Customizing Aspect Ratio

Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 5 selections of Ymux for the same Words and the same Bpw SPSRAMA. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of SPSRAM, In general, larger Ymux SPSRAMA has faster speed and bigger area than smaller Ymux SPSRAMA.

3) Selecting Number of Banks

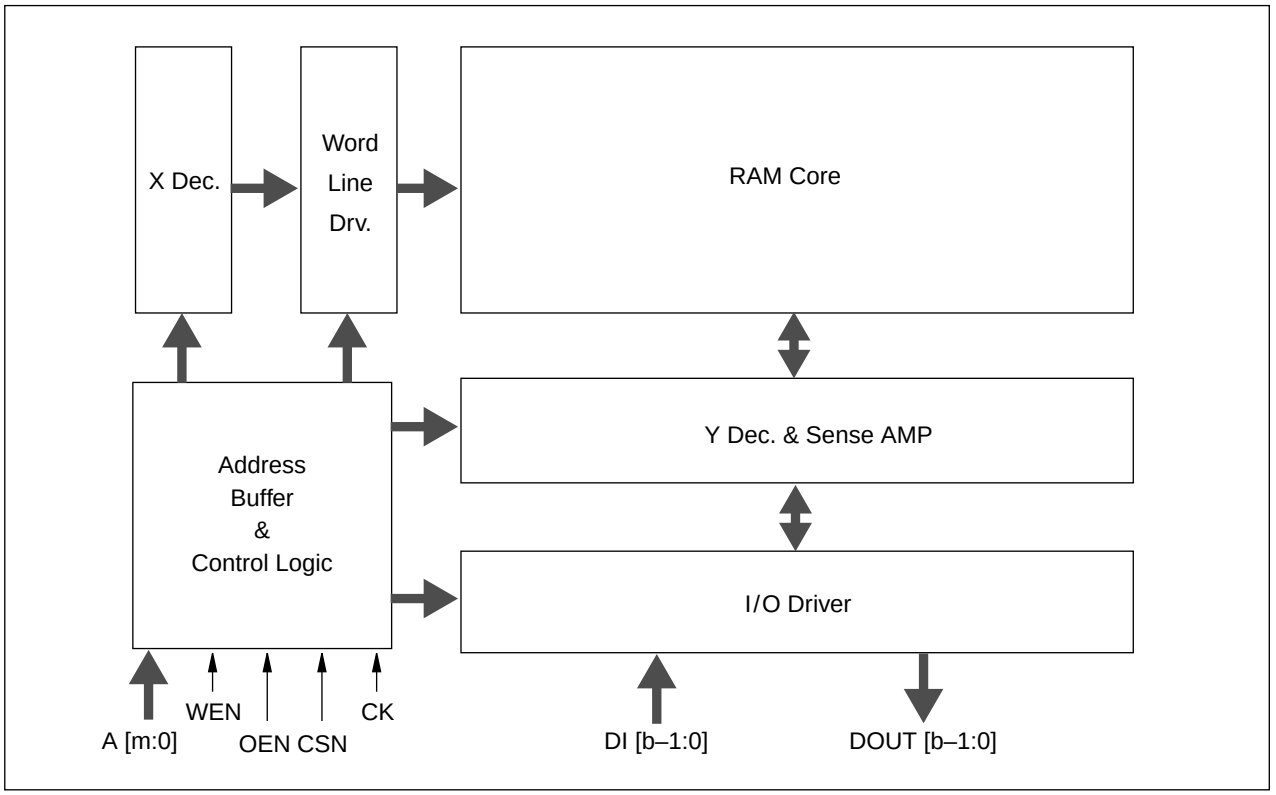
To enlarge the capacity of SPSRAMA, we added one more option to choose number of banks. If you want to use larger SPSRAMA than 64K bit SPSRAMA, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 64K bit SPSRAMA. Dual bank SPSRAMA is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

4) Using Bi-Directional Data Port

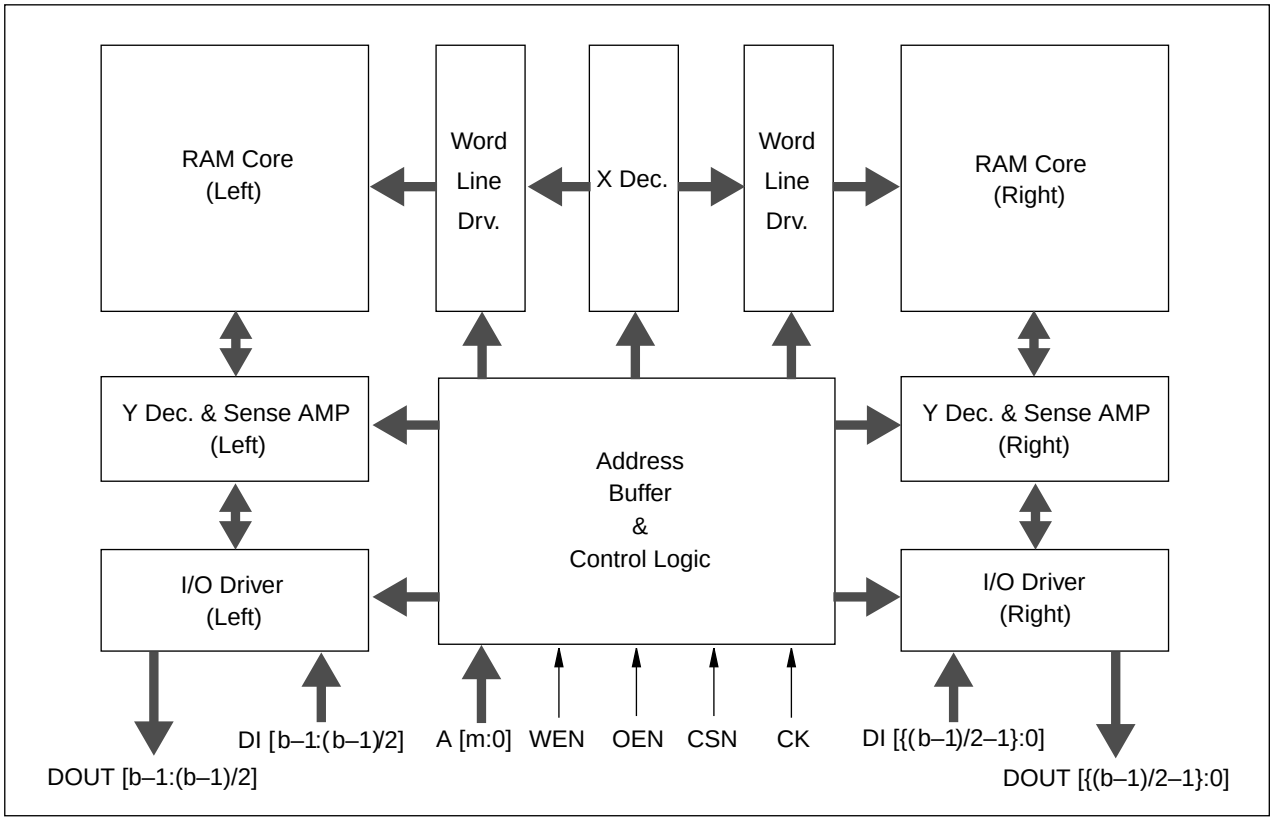
Because having the same phase, DI [ ] and DOUT [ ] of SPSRAMA can be tied directly. With tying them up together and controlling WEN and OEN properly, you can use them as bi-directional data ports.

Block Diagrams

< 1-bank >



< 2-bank >



Characteristic Reference Table

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)							
t_{rp}	Minimum Read Pulse Width	6.55	6.47	7.10	6.90	8.20	7.90
t_{pc}	Minimum Pre-Charge Period	2.73	2.52	3.90	3.40	6.20	5.30
t_{wp}	Minimum Write Pulse Width	1.20	1.20	1.52	1.55	2.10	2.20
t_{as}	Address Setup Time	0.44	0.44	0.63	0.63	1.03	1.02
t_{ah}	Address Hold Time	0.97	0.92	1.20	1.00	1.64	1.41
t_{cs}	CSN Setup Time	0.51	0.51	0.51	0.51	0.51	0.51
t_{ch}	CSN Hold Time	0	0	0	0	0	0
t_{ds}	Data Input Setup Time	0.68	0.75	0.91	1.00	1.36	1.61
t_{dh}	Data Input Hold Time	1.74	1.59	2.04	1.75	2.66	2.00
t_{os}	OEN Setup Time	0	0	0	0	0	0
t_{oh}	OEN Hold Time	1.36	1.33	1.50	1.40	1.78	1.66
t_{wh}	WEN Hold Time	0.74	0.72	0.79	0.74	0.88	0.79
t_{acc}	Access Time	4.50	0.43	5.10	0.48	6.20	5.80
t_{da}	Deaccess Time	2.10	1.90	2.30	2.00	2.60	2.10
SIZE (µm)							
Width		622	703	1131	1212	2142	2222
Height		902	902	1501	1501	2697	2697
POWER (µW/MHz)							
power_ck (normal mode: CSN Low)		717		1816		5318	
power_csn (stand-by mode: CSN High)		48		93		197	

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
B: Bits per Word
Y: Ymux Type
BA: Number of Banks (1 or 2)
S: Input Slope (Unit: ns)
SL: Number of Fanouts (Unit: Standard Load)
VDD: Operating Voltage (Unit: V)
F: Operating Frequency (Unit: MHz)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
tpc	5.79e – 03 * W + 1.31e – 02 * B / BA + 3.48e – 01 * S + 1.1579
trp	3.14e – 03 * W + 4.71e – 03 * B / BA – 3.02e – 01 * S + 1.4025 * 0.02 * SL + 2.3669
tacc	2.82e – 03 * W + 6.89e – 03 * B / BA + 5.39e – 01 * 0.02 * SL + 2.3079
	Y = 4
tpc	2.89e – 03 * W + 2.63e – 02 * B / BA + 3.48e – 01 * S + 1.1579
trp	1.57e – 03 * W + 9.42e – 03 * B / BA – 3.02e – 01 * S + 1.4025 * 0.02 * SL + 2.3669
tacc	1.41e – 03 * W + 1.37e – 02 * B / BA + 5.39e – 01 * 0.02 * SL + 2.3079
	Y = 8
tpc	1.44e – 03 * W + 5.26e – 02 * B / BA + 3.48e – 01 * S + 1.1579
trp	7.85e – 04 * W + 1.88e – 02 * B / BA – 3.02e – 01 * S + 1.4025 * 0.02 * SL + 2.3669
tacc	7.06e – 04 * W + 2.75e – 02 * B / BA + 5.39e – 01 * 0.02 * SL + 2.3079
	Y = 16
tpc	7.23e – 04 * W + 1.05e – 01 * B / BA + 3.48e – 01 * S + 1.1579
trp	3.92e – 04 * W + 3.76e – 02 * B / BA – 3.02e – 01 * S + 1.4025 * 0.02 * SL + 2.3669
tacc	3.53e – 04 * W + 5.51e – 02 * B / BA + 5.39e – 01 * 0.02 * SL + 2.3079
	Y = 32
tpc	3.61e – 04 * W + 2.10e – 01 * B / BA + 3.48e – 01 * S + 1.1579
trp	1.96e – 04 * W + 7.53e – 02 * B / BA – 3.02e – 01 * S + 1.4025 * 0.02 * SL + 2.3669
tacc	1.76e – 04 * W + 1.10e – 01 * B / BA + 5.39e – 01 * 0.02 * SL + 2.3079

2) Power Characteristics [Unit: μW]

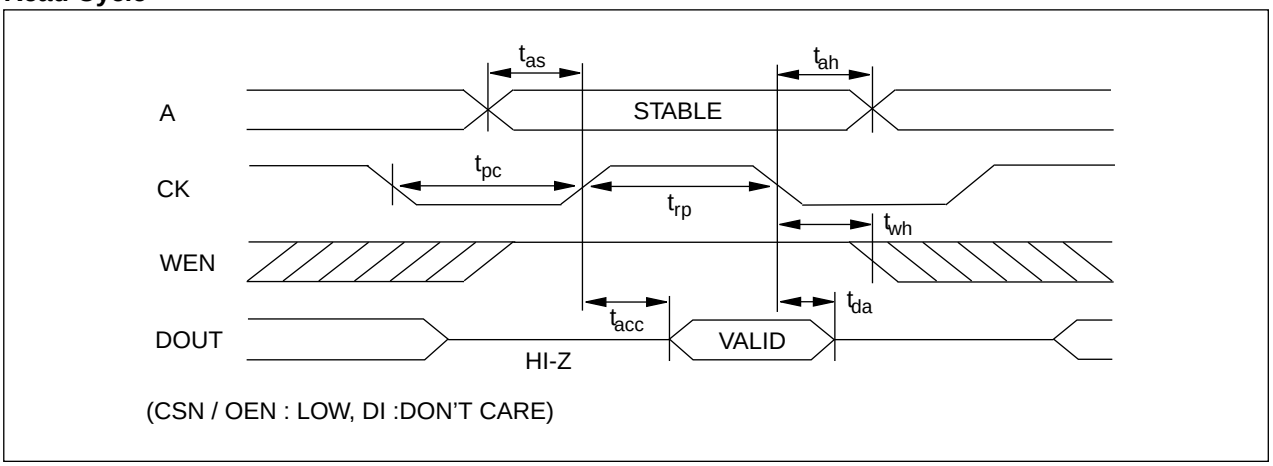
Power Type	Power Equation
	Y = 2
power_ck	(1.6311e – 01 * W + 6.2978e – 01 * B + 4.9380 + 4.8722e – 03 * W * B) * VDD^2 * F
power_csn	(3.7429e – 03 * W + 9.8542e – 02 * B + 5.8775e – 01 + 4.6534e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(8.1556e – 02 * W + 1.2595 * B + 4.9380 + 4.8722e – 03 * W * B) * VDD^2 * F
power_csn	(1.8714e – 03 * W + 1.9708e – 01 * B + 5.8775e – 01 + 4.6534e – 05 * W * B) * VDD^2 * F
	Y = 8
power_ck	(4.0778e – 02 * W + 2.5191 * B + 4.9380 + 4.8722e – 03 * W * B) * VDD^2 * F
power_csn	(9.3573e – 04 * W + 3.9417e – 01 * B + 5.8775e – 01 + 4.6534e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(2.0389e – 02 * W + 5.0382 * B + 4.9380 + 4.8722e – 03 * W * B) * VDD^2 * F
power_csn	(4.6786e – 04 * W + 7.8834e – 01 * B + 5.8775e – 01 + 4.6534e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(1.0194e – 02 * W + 1.0076e + 01 * B + 4.9380 + 4.8722e – 03 * W * B) * VDD^2 * F
power_csn	(2.3393e – 04 * W + 1.5766 * B + 5.8775e – 01 + 4.6534e – 05 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 6 * ($\lceil \log_2 (W / Y) \rceil$) + 76.3 * BA + 4.4 (B * Y / 4 + BA) + 6.75 * B * Y + 2.25 [μm]
Height = 297.5 + 9.35 * W / Y + M [μm]
M = 5.75 (if Y = 2, 4, 8, 16), M = 8.15 (if Y = 32)

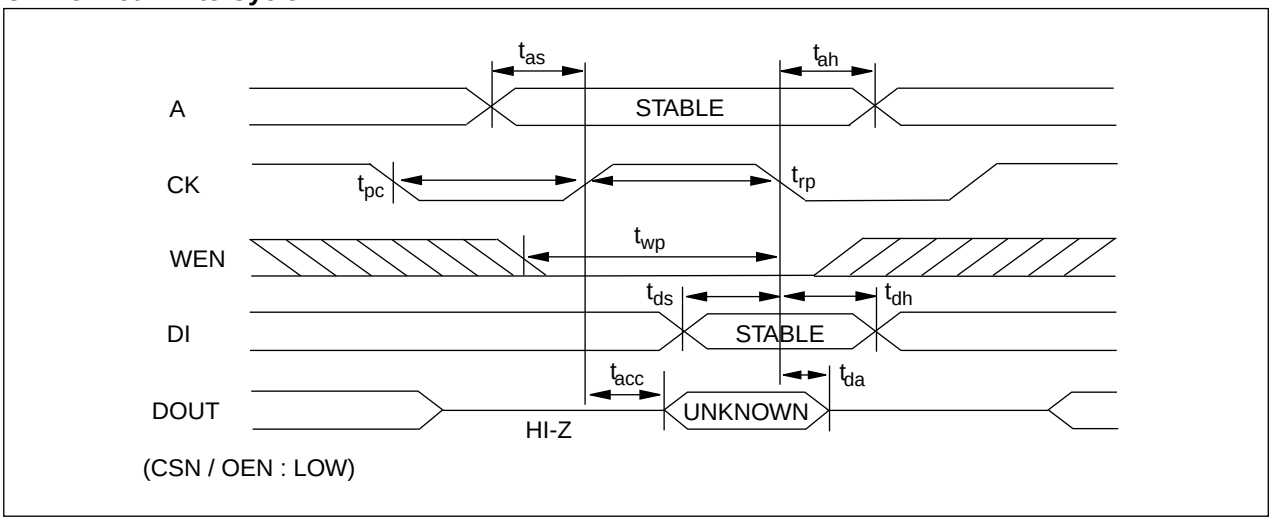
Timing Diagrams

Read Cycle

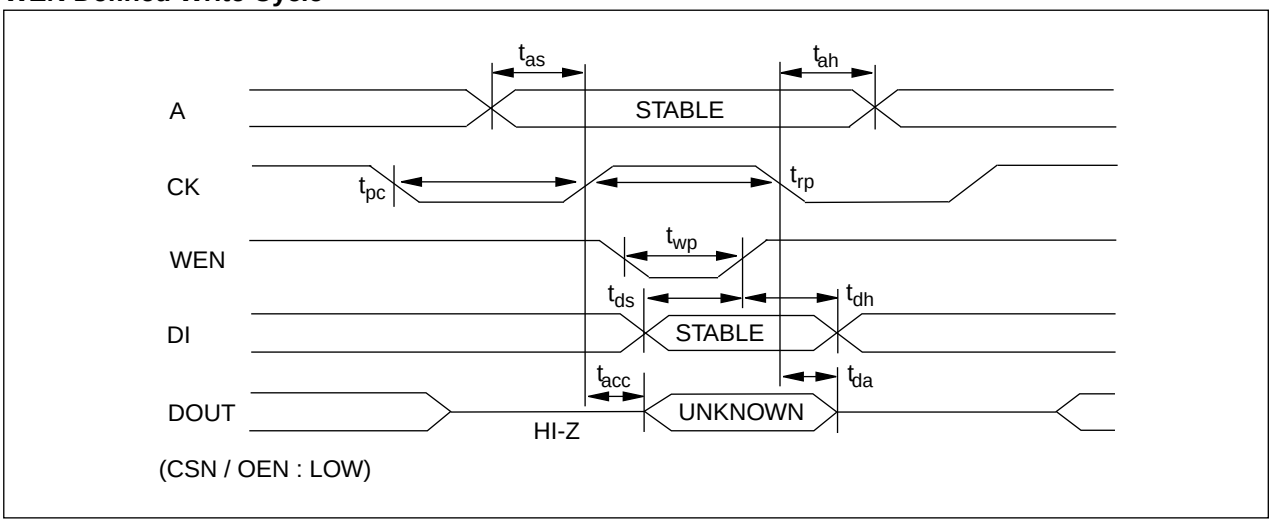


(CSN / OEN : LOW, DI :DON'T CARE)

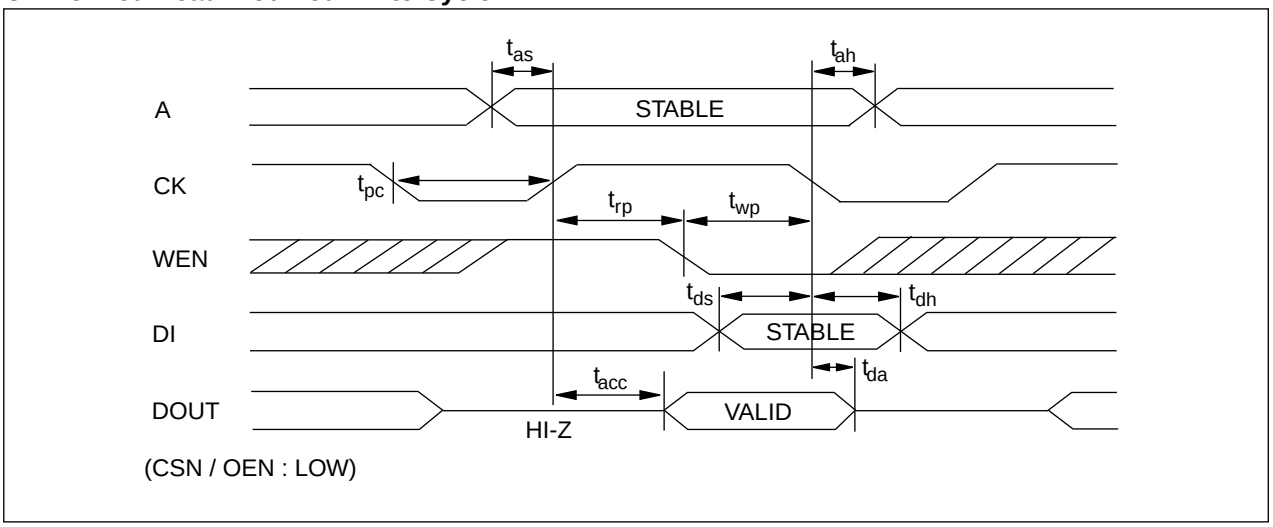
CK Defined Write Cycle



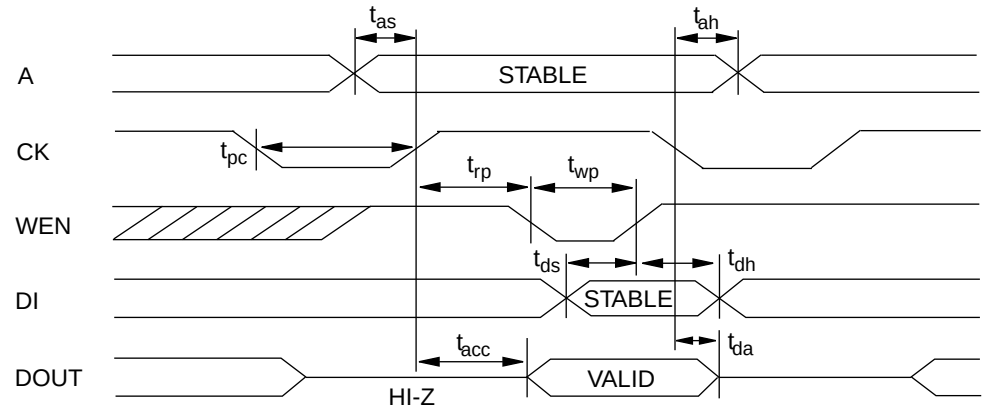
WEN Defined Write Cycle



CK Defined Read-Modified-Write Cycle

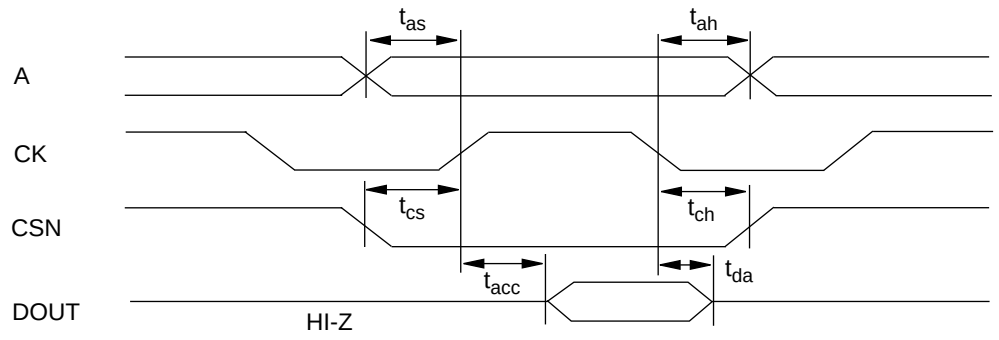


WEN Defined Read-Modified-Write Cycle



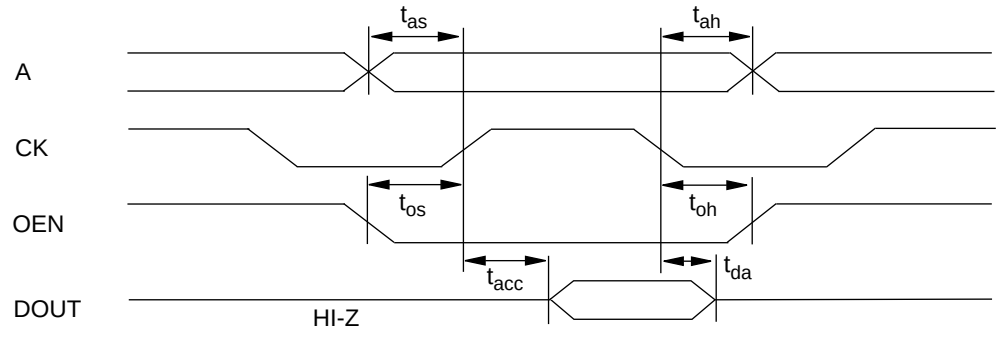
(CSN / OEN : LOW)

CSN Control



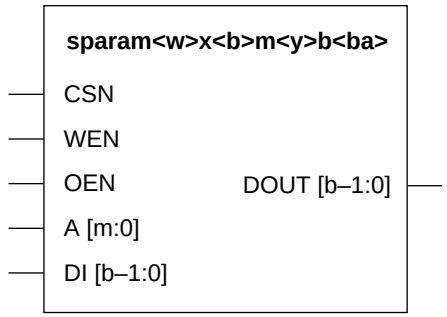
(OEN : LOW, WEN / DI : DON'T CARE)

OEN Control



(CSN : LOW, WEN / DI : DON'T CARE)

Logic Symbol



NOTES:

1. Words (w) is the number of words in SPARAM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. Banks (ba) is the number of banks.
5. $m = \lceil \log_2 w \rceil - 1$

Features

- Asynchronous operation
- Address transition detectors
- Write enable transition detector
- Chip select transition detector
- Stand-by (power down) mode available
- Data output latching
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Flexible aspect ratio
- Optional dual bank capacity
- Up to 128K bits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

SPARAM is a single-port asynchronous static RAM. When WEN is high, just after the address (A [ ]) transition, DOUT [ ] presents data stored in the location addressed by A [ ]. Upon WEN rising edge, the value of DI [ ] is written into the location addressed by A [ ]. CSN is used to enable/disable the access. OEN is used to enable/disable the data output driver.

Generators and Cell Configurations

SPARAM Gen. generates layout, netlist, symbol and functional & timing model of SPARAM. The layout of SPARAM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of SPARAM, you can give certain values to following four generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y)
- Number of banks (ba).

The valid range of these parameters is specified in the following table:

Parameters			YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)		Min	16	32	64	128
		Max	1024	2048	4096	8192
		Step	8	16	32	64
Bpw (b)	ba = 1	Min	1	1	1	1
		Max	64	32	16	8
		Step	1	1	1	1
	ba = 2	Min	2	2	2	2
		Max	128	64	32	16
		Step	1	1	1	1

SPARAM Gen

Single-Port Asynchronous RAM Generator

Pin Descriptions

Name	I/O	Description
CSN	I	“Chip Select Negative” acts as the memory enable signal for selections of multiple blocks on a common clock. When CSN is high, the memory goes to stand-by (power down) mode and no access to the memory can occur, conversely, if low only then may a read or write access occur. When CSN falls, an access is initiated. When CSN rises, a write access is completed if WEN is low.
WEN	I	“Write Enable Negative” selects the type of memory access. Read is the high state, and write is the low state. Upon the rising edge of WEN, a write access completed and a read access initiated.
OEN	I	“Output Enable Negative” unconditionally controls the output drivers from driven to tri-state condition.
A [ ]	I	“Address” selects the location to be accessed. When “Address” changes, the transition is detected and the internal clock pulse will be generated.
DI [ ]	I	When WEN rises, the “Data In” word value is written to the accessed location.
DOUT [ ]	O	During a read access, data word stored will be presented to the “Data Out” ports. DOUT [ ] is tri-statable. When CSN is low and OEN is low, only then, DOUT [ ] drives a certain value. Otherwise, DOUT [ ] keeps Hi-Z state. During a write access, data on DOUT [ ] is unpredictable.

Pin Capacitance

(Unit = SL)

	CSN	WEN	OEN	A	DI	DOUT			
						Ymux 4	Ymux 8	Ymux 16	Ymux 32
1-bank	9.7	4.2	0.7	4.2	1.9	5.5	11.7	24.1	49.0
2-bank	19.3	8.4	1.3	4.2	1.9	5.5	11.7	24.1	49.0

Application Notes

1) Customizing Aspect Ratio

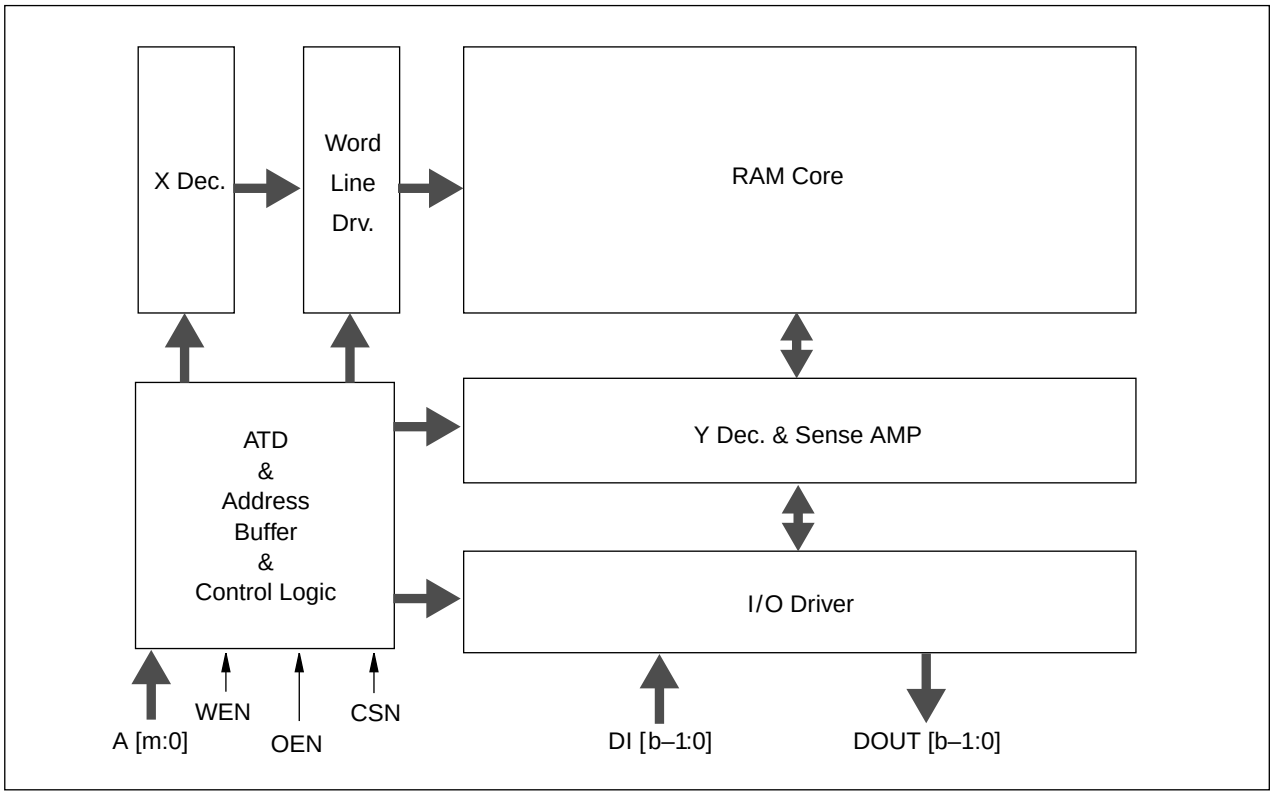
Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 4 selections of Ymux for the same Words and the same Bpw SPARAM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of SPARAM, In general, larger Ymux SPARAM has faster speed and bigger area than smaller Ymux SPARAM.

2) Selecting Number of Banks

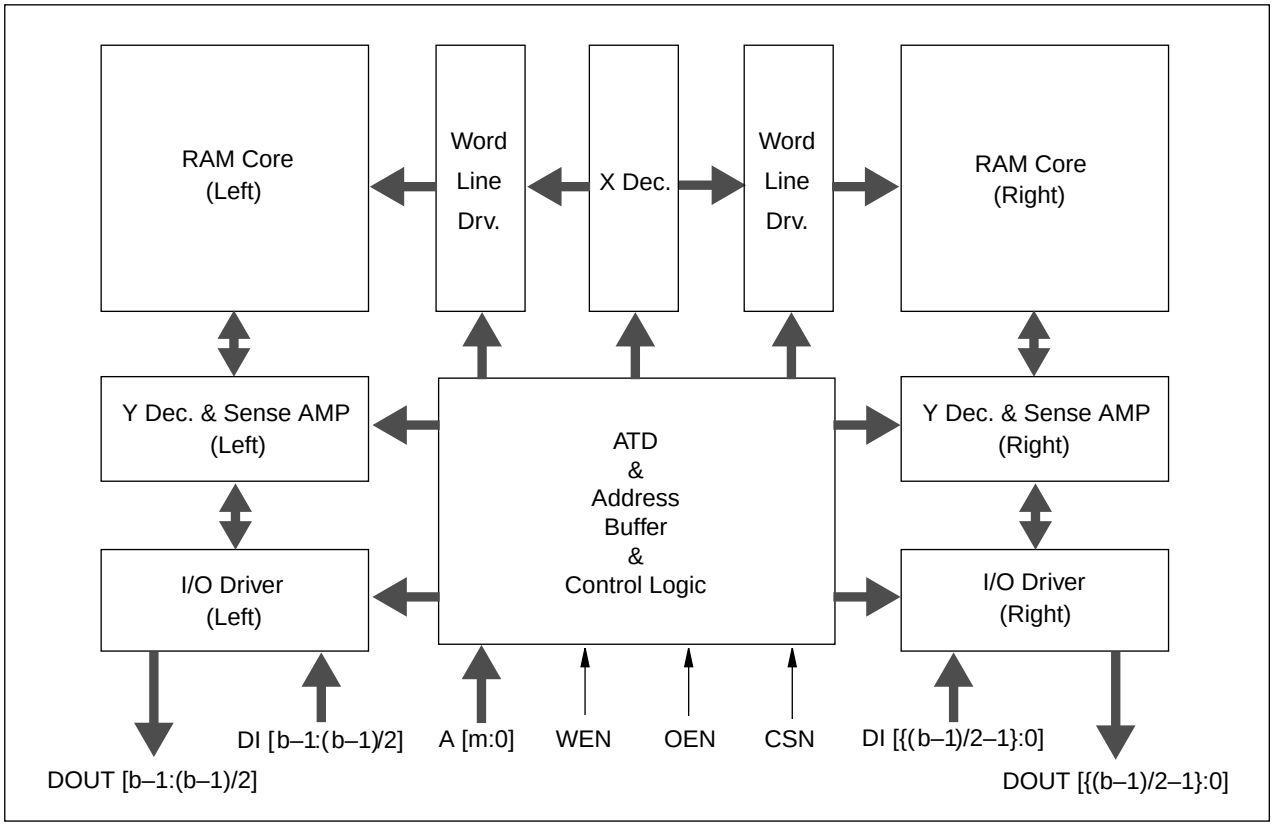
To enlarge the capacity of SPARAM, we added one more option to choose number of banks. If you want to use larger SPARAM than 64K bit SPARAM, you can select dual bank (ba = 2). You can also select dual bank for smaller one than 64K bit SPARAM. Dual bank SPARAM is a little bigger and a little faster than single bank one. (Please refer to the characteristic tables.)

Block Diagrams (1 Bank)

< 1-bank >



< 2-bank >



Characteristic Reference Table

Symbol	Description	256x16m4		1024x16m8		4Kx16m16	
		1-ba	2-ba	1-ba	2-ba	1-ba	2-ba
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{O}C, Output load = 10SL, Unit = ns)							
t_{as}	Address Setup Time	0	0	0	0	0	0
t_{ah}	Address Hold Time	0	0	0	0	0	0
t_{cs}	CSN Setup Time	5.70	5.70	6.10	6.10	6.80	6.80
t_{ch}	CSN Hold Time	5.70	5.70	6.10	6.10	6.80	6.80
t_{ds}	Data Input Setup Time	0.80	0.90	0.80	1.00	0.80	1.20
t_{dh}	Data Input Hold Time	0.70	0.60	0.90	0.70	1.20	0.80
t_{acc}	Access Time	6.10	6.10	6.30	6.30	6.80	6.80
t_{da}	Deaccess Time	0.70	0.70	0.70	0.70	0.70	0.70
t_{csn}	Minimum CSN Pulse Width for Write cycle	5.70	5.70	6.10	6.10	6.80	6.80
t_{wen}	Minimum WEN Pulse Width for Write Cycle	5.70	5.70	6.10	6.10	6.80	6.80
t_{od}	OEN to Valid Output	1.80	1.80	1.80	1.80	1.80	1.80
t_{dz}	Valid Data to Hi-Z	1.80	1.80	1.80	1.80	1.80	1.80
t_{zd}	Hi-Z to Valid Data	0.73	0.73	0.73	0.73	0.73	0.73
mincyc	Minimum Address Cycle Time	6.10	6.10	6.30	6.30	6.80	6.80
SIZE (μm)							
Width		723	891	1206	1374	2172	2340
Height		972	972	1577	1577	2786	2786
POWER (μW/MHz)							
power_add (normal mode: CSN Low)			1418		2776		6370
power_csn (stand-by mode: CSN High)			228		435		827

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
BA: Number of Banks (1 or 2)
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 4
mincyc	(9.1927e – 04 * W + 6.2820e – 02 * S + 1.3449e – 01 * 0 02 * SL + 5.7726)
tacc	(9.1927e – 04 * W + 6.2820e – 02 * S + 1.3449e – 01 * 0 02 * SL + 5.7726)
twen	(1.9796e – 03 * W + 7.9464e – 01 * S + 4.4018 – 4.7763e – 04 * W * S)
	Y = 8
mincyc	(4.5963e – 04 * W + 6.2820e – 02 * S + 1.3449e – 01 * 0.02 * SL +5.7726)
tacc	(4.5963e – 04 * W + 6.2820e – 02 * S + 1.3449e – 01 * 0.02 * SL +5.7726)
twen	(9.8983e – 04 * W + 7.9464e – 01 * S + 4.4018 – 2.3881e – 04 * W * S)
	Y = 16
mincyc	(2.2981e – 04 * W + 6.2820e – 02 * S + 1.3449e – 01 * 0.02 * SL + 5.7726)
tacc	(2.2981e – 04 * W + 6.2820e – 02 * S + 1.3449e – 01 * 0.02 * SL + 5.7726)
twen	(4.9491e – 04 * W + 7.9464e – 01 * S + 4.4018 – 1.1940e – 04 * W * S)
	Y = 32
mincyc	(1.1490e – 04 * W + 6.2820e – 02 * S + 1.3449e – 01 * 0.02 * SL + 5.7726)
tacc	(1.1490e – 04 * W + 6.2820e – 02 * S + 1.3449e – 01 * 0.02 * SL + 5.7726)
twen	(2.4745e – 04 * W + 7.9464e – 01 * S + 4.4018 – 5.9704e – 05 * W * S)

2) Power Characteristics [Unit: μW]

Power Type	Power Equation
	Y = 4
power_add	(3.0602e – 02 * W + 3.8308 * B + 4.0483e + 01 + 5.0528e – 03 * W * B) * VDD^2 * F
power_csn	(1.6749e – 02 * W + 9.3084e – 01 * B + 2.4629 – 4.7554e – 05 * W * B) * VDD^2 * F
	Y = 8
power_add	(9.9226e – 03 * W + 6.2904 * B + 4.0384e + 01 + 6.3934e – 03 * W * B) * VDD^2 * F
power_csn	(8.3748e – 03 * W + 1.8616 * B + 2.4629 – 4.7554e – 05 * W * B) * VDD^2 * F
	Y = 16
power_add	(6.0183e – 03 * W + 1.3309e + 01 * B + 4.3131e + 01 + 4.6519e – 03 * W * B) * VDD^2 * F
power_csn	(4.1874e – 03 * W + 3.7233 * B + 2.4629 – 4.7554e – 05 * W * B) * VDD^2 * F
	Y = 32
power_add	(2.0329e – 03 * W + 2.6417e + 01 * B + 4.6469e + 01 + 4.7973e – 03 * W * B) * VDD^2 * F
power_csn	(2.0937e – 03 * W + 7.4467 * B + 2.4629 – 4.7554e – 05 * W * B) * VDD^2 * F

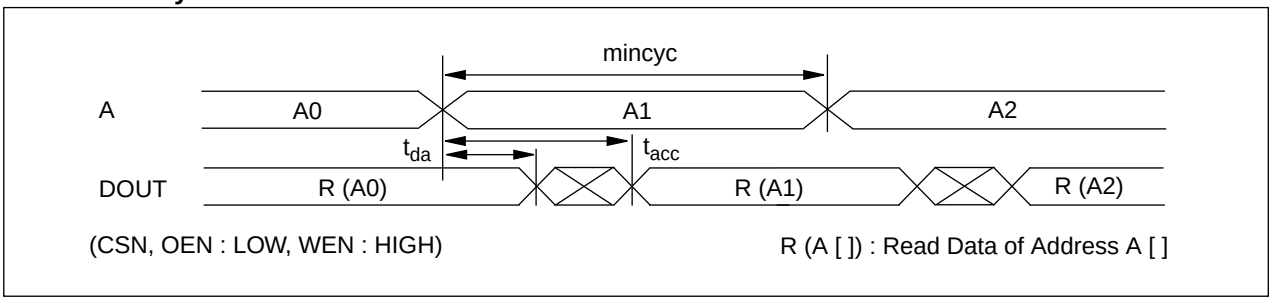
3) Size Equation [Unit: μm]

Width = 12 * ($\lceil \log_2 (W / Y) \rceil$) + 170 * BA + 7.55 * (B * Y) – 5 [μm]

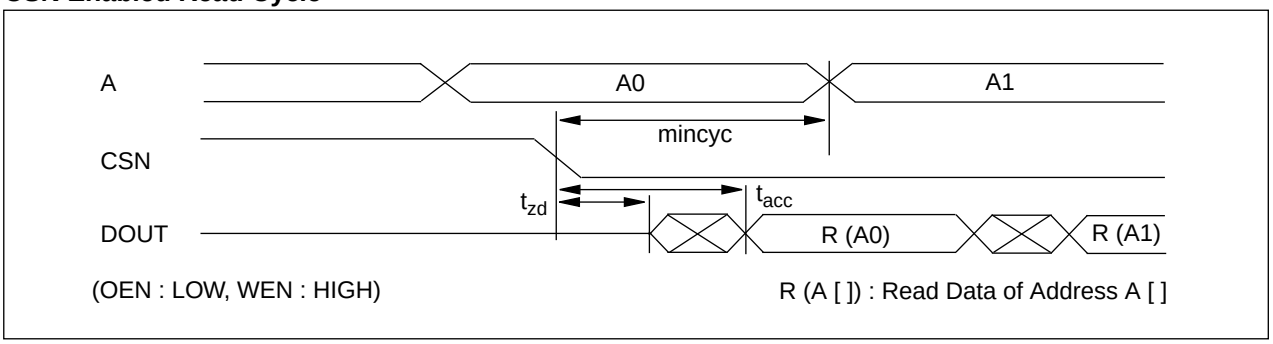
Height = 366.7 + 9.45 * W / Y [μm]

Timing Diagrams

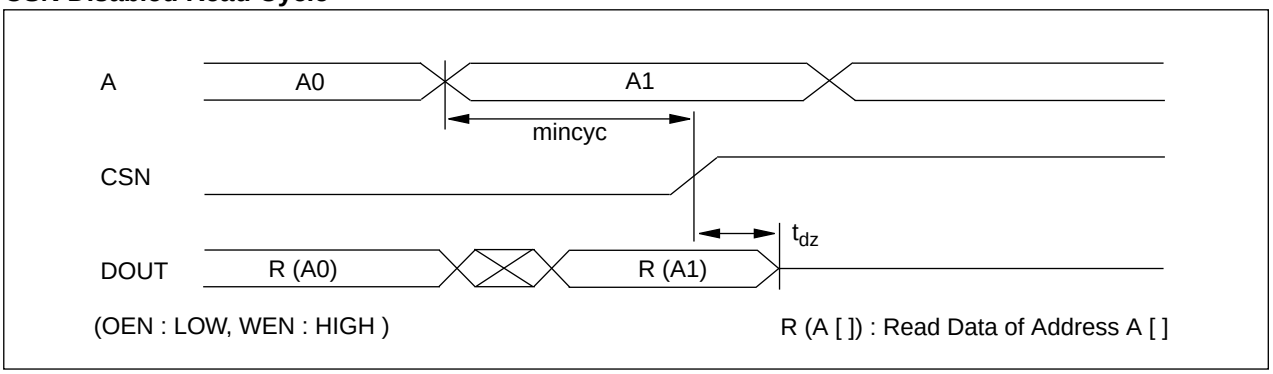
Basic Read Cycle



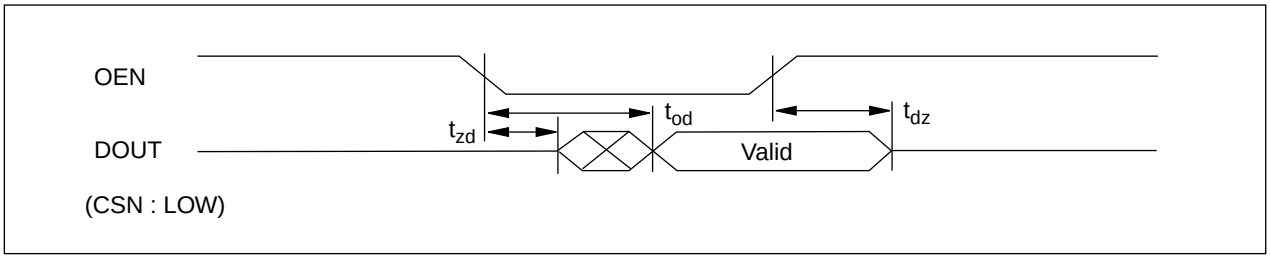
CSN Enabled Read Cycle



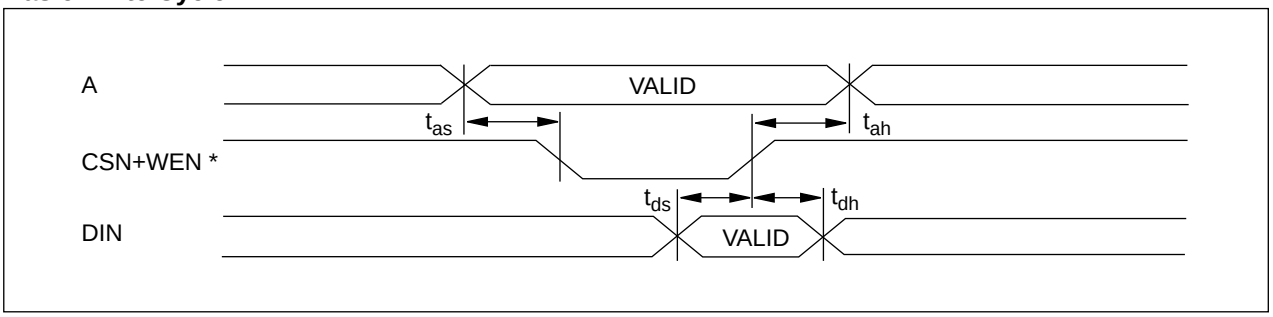
CSN Disabled Read Cycle



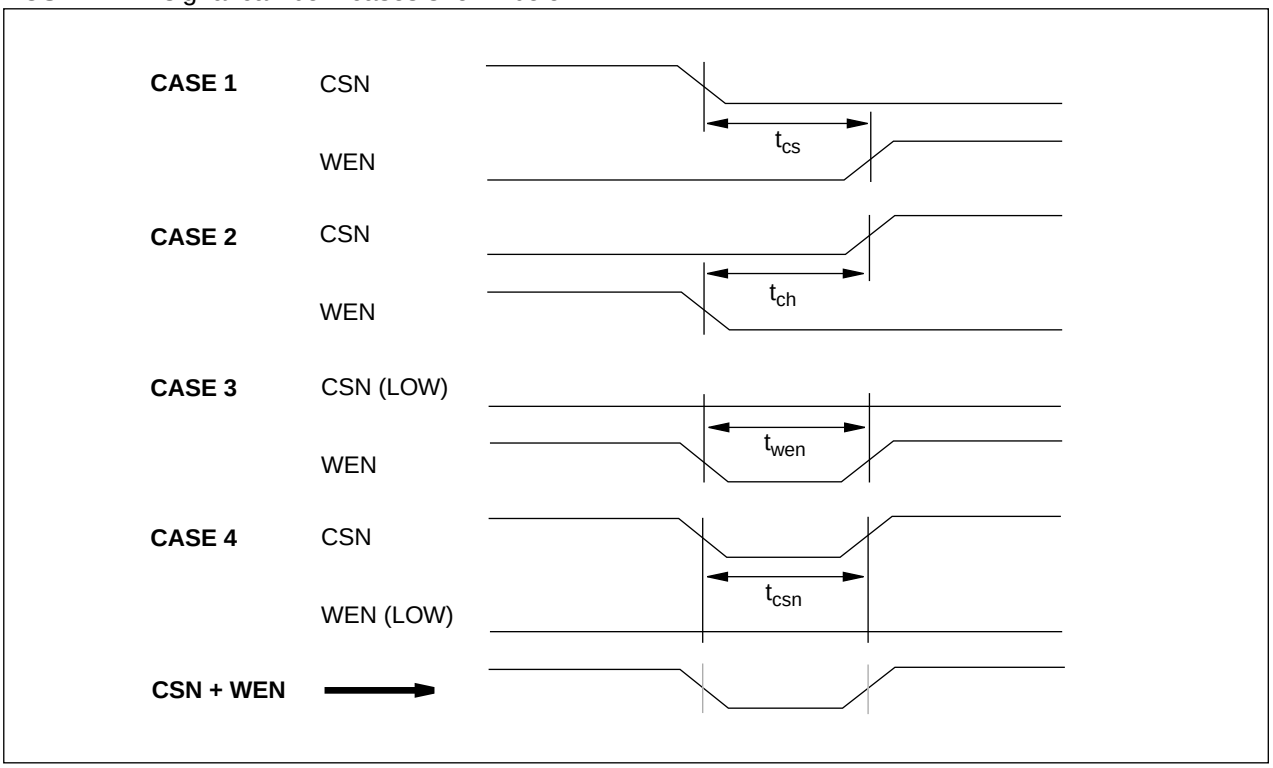
OEN Controlled



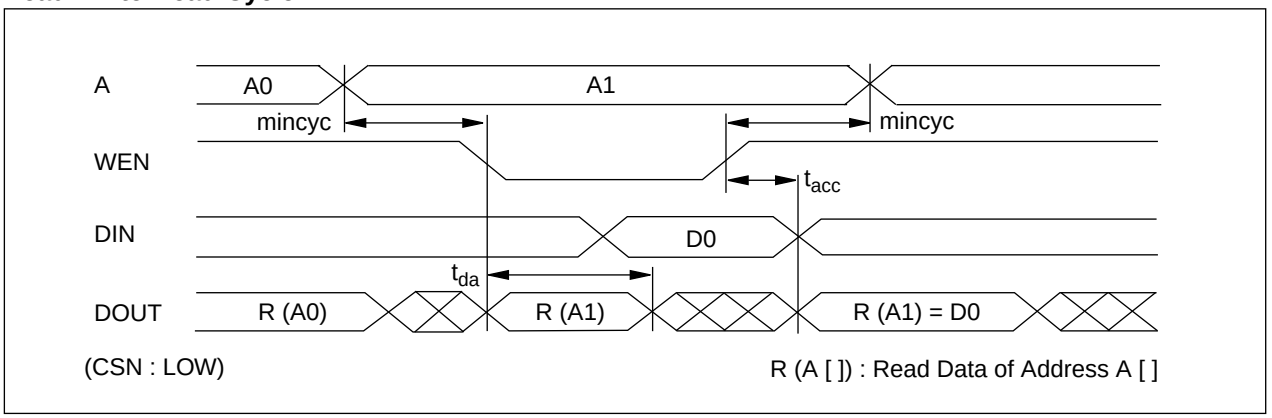
Basic Write Cycle



* CSN+WEN signal can be 4 cases shown below.



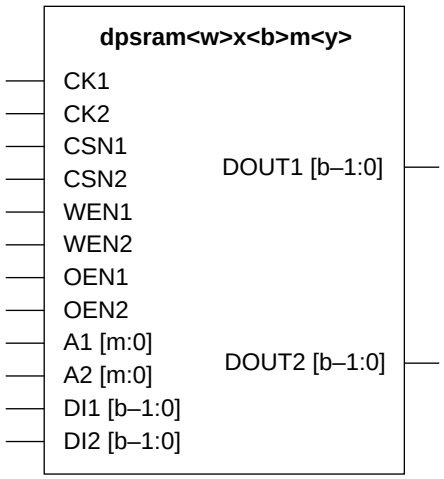
Read-Write-Read Cycle



DPSRAM Gen

Dual-Port Synchronous RAM Generator

Logic Symbol



NOTES:

1. Words (w) is the number of words in DPSRAM.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Write completed at rising edge of clock
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Flexible aspect ratio
- Up to 64K bits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

DPSRAM is a dual-port synchronous static RAM. When CK1 rises, if WEN1 is high, DOUT1 [ ] presents data stored in the location addressed by A1 [ ], otherwise the value of DI1 [ ] is written into the location addressed by A1 [ ]. CSN1 is used to enable/disable CK1. OEN1 is used to enable/disable tri-state drivers of DOUT1 [ ]. The functionality of port2 is the same to port1. The port1 and port2 function independently each other.

Generators and Cell Configurations

DPSRAM Gen. generates layout, netlist, symbol and functional & timing model of DPSRAM. The layout of DPSRAM is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of DPSRAM, you can give certain values to following three generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y).

The valid range of these parameters is specified in the following table:

Parameters		YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	Min	4	8	16	32	64
	Max	512	1024	2048	4096	8192
	Step	2	4	8	16	32
Bpw (b)	Min	1	1	1	1	1
	Max	128	64	32	16	8
	Step	1	1	1	1	1

Pin Descriptions

Name	I/O	Description
CK1 CK2	I	“Clock”s serve as input clocks to each port of the memory block. When CK1 (CK2) is low, port1 (port2) is in a precharge state. Upon the rising edge, an access begins.
CSN1 CSN2	I	“Chip Select Negative”s act as each port’s enable signal for selections of multiple blocks on a common clock. When CSN1 (CSN2) is high, port1 (port2) goes to stand-by (power down) mode and no access can occur, conversely, if low only then may a read or write access occur. CSN1 (CSN2) may not change during CK1 (CK2) is high.
WEN1 WEN2	I	“Write Enable Negative”s select the type of memory access. Read is the high state, and write is the low state.
OEN1 OEN2	I	“Output Enable Negative”s control the output drivers from driven to tri-state condition. OEN1 (OEN2) may not change during CK1 (CK2) is high.
A1 [ ] A2 [ ]	I	“Address”es select the location to be accessed. A1 [ ] (A2 [ ]) may not change during CK1 (CK2) is high.
DI1 [ ] DI2 [ ]	I	When CK1 (CK2) rises while WEN1 (WEN2) is low, the “Data In” word value is written to the accessed location.
DOUT1 [ ] DOUT2 [ ]	O	During a read access, data word stored will be presented to the “Data Out” ports. DOUT1 [ ] and DOUT2 [ ] are tri-statable. Only when CK1 (CK2) is high, CSN1 (CSN2) and OEN1 (OEN2) is low, DOUT1 [ ] (DOUT2 [ ]) drives a certain value. Otherwise, DOUT1 [ ] (DOUT2 [ ]) keeps Hi-Z state. During a write access, data word written will be presented at the “Data Out” ports if output driver is enabled.

Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	DI	DOUT				
						Ymux 2	Ymux 4	Ymux 8	Ymux 16	Ymux 32
5.8	1.9	0.9	2.3	1.0	2.0	5.4	5.4	12.0	25.0	51.0

Application Notes

1) Putting Busholders on DOUT1 [ ] and DOUT2 [ ]

As you will see in the timing diagrams, DOUT1 [ ] (DOUT2 [ ]) is valid only when CK1 (CK2) is high. If you want DOUT1 [ ] (DOUT2 [ ]) to be stable regardless of CK1 (CK2) state, you should put STDL80 Busholder cells on the DOUT1 [ ] (DOUT2 [ ]) bus externally.

2) Customizing Aspect Ratio

Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 5 selections of Ymux for the same Words and the same Bpw DPSRAM. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of DPSRAM, In general, larger Ymux DPSRAM has faster speed and bigger area than smaller Ymux DPSRAM.

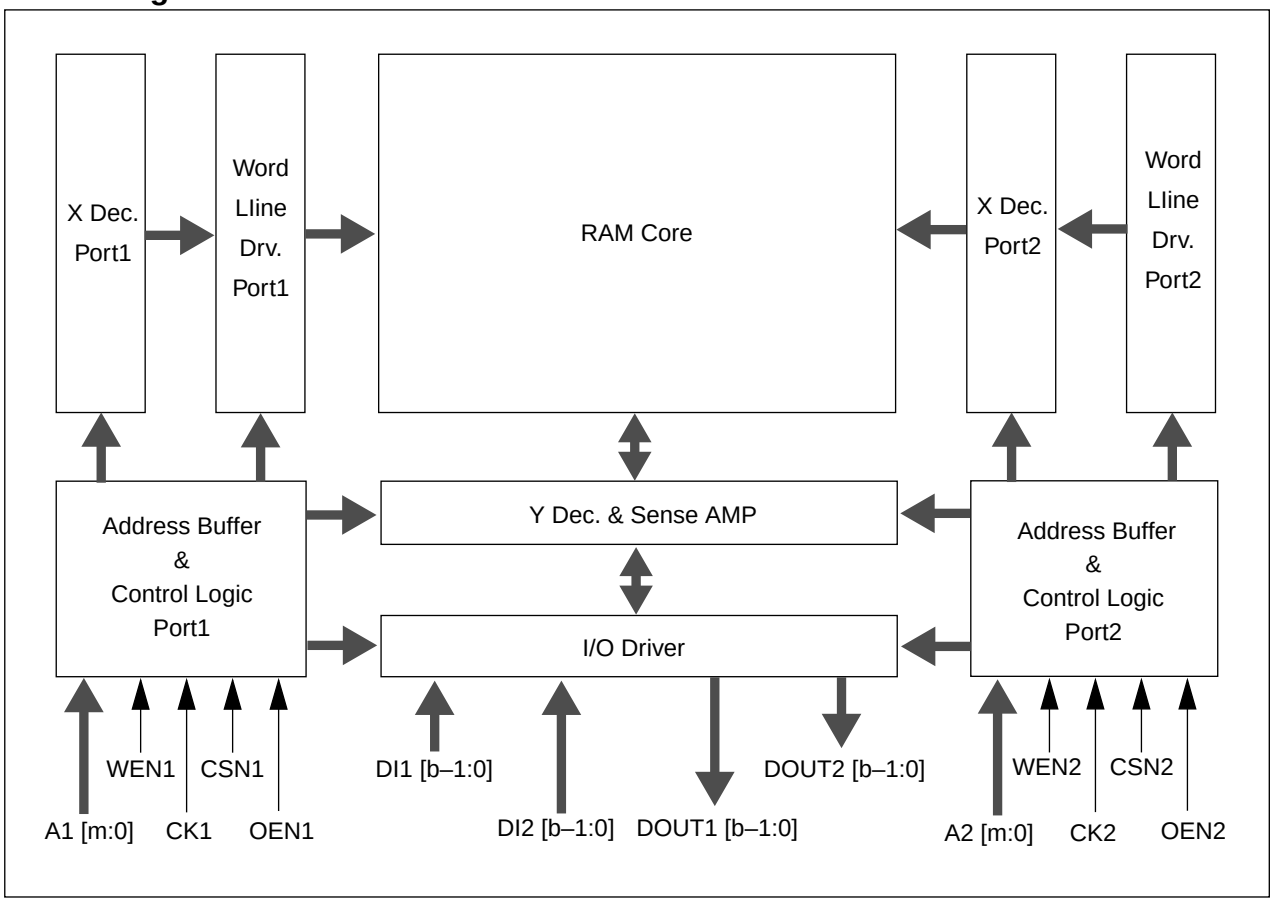
3) Contention Modes

Simultaneous accesses to the same location through both ports cause a contention. DPSRAM has no contention preventing scheme. You have to take care of the contention modes. Please refer to the timing diagrams of contention modes to get more information of contention modes.

DPSRAM Gen

Dual-Port Synchronous RAM Generator

Block Diagram



Characteristic Reference Table

Symbol	Description	256x16m4	1024x16m8	4Kx16m16
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{o}C, Output load = 10SL, Unit = ns)				
minckl	Minimum Clock Pulse Width Low	2.30	2.90	4.10
minckh	Minimum Clock Pulse Width High	4.00	4.60	5.70
t_{cc}	Clock to Clock Setup Time	3.20	4.30	6.40
t_{as}	Address Setup Time	0.31	0.55	0.96
t_{ah}	Address Hold Time	0.43	0.43	0.42
t_{cs}	CSN Setup Time	0.52	0.52	0.52
t_{ch}	CSN Hold Time	0	0	0
t_{ds}	Data Input Setup Time	0	0	0
t_{dh}	Data Input Hold Time	3.30	4.30	5.60
t_{os}	OEN Setup Time	0	0	0
t_{oh}	OEN Hold Time	1.45	1.60	1.83
t_{ws}	WEN Setup Time	0	0	0
t_{wh}	WEN Hold Time	0	0	0
t_{acc}	Access Time	3.40	4.00	5.30
t_{da}	Deaccess Time	1.90	2.00	2.40
mincyc	Minimum Clock Cycle Time	7.00	9.60	14.60
SIZE (μm)				
Width		996	1787	3353
Height		1110	1802	3194
POWER (μW/MHz)				
power_ck (normal mode: CSN Low)		805	1675	4094
power_csn (stand-by mode: CSN High)		118	217	370

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
B: Bits per Word
Y: Ymux Type
SL: Number of Fanouts (Unit: Standard Load)
S: Input Slope (Unit: ns)
F: Operating Frequency (Unit: MHz)
VDD: Operating Voltage (Unit: V)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
mincyc	(1.6027e – 02 * W + 7.7418e – 03 * B + 2.3100e – 01 * 0.02 * SL + 3.4424) * 1.1
minckh	(2.5018e – 03 * W + 4.0217e – 03 * B + 6.0637e – 01 * 0.02 * SL + 1.8118)
minckl	(3.3328e – 03 * W + 5.7062e – 03 * B + 1.6429 + 9.4074e – 07 * W * B)
tacc	(3.0738e – 03 * W + 7.8335e – 03 * B + 1.4519e – 01 * S + 3.0153e – 01 * 0.02 * SL + 2.4784)
	Y = 4
mincyc	(8.0139e – 03 * W + 1.5483e – 02 * B + 2.3100e – 01 * 0.02 * SL + 3.4424) * 1.1
minckh	(1.2509e – 03 * W + 8.0434e – 03 * B + 6.0637e – 01 * 0.02 * SL + 1.8118)
minckl	(1.6664e – 03 * W + 1.1412e – 02 * B + 1.6429 + 9.4073e – 07 * W * B)
tacc	(1.5369e – 03 * W + 1.5667e – 02 * B + 1.4519e – 01 * S + 3.0153e – 01 * 0.02 * SL + 2.4784)
	Y = 8
mincyc	(4.0069e – 03 * W + 3.0967e – 02 * B + 2.3100e – 01 * 0.02 * SL + 3.4424) * 1.1
minckh	(6.1447e – 04 * W + 1.5623e – 02 * B + 6.3323e – 01 * 0.02 * SL + 1.9109)
minckl	(8.3320e – 04 * W + 2.2825e – 02 * B + 1.6429 + 9.4074e – 07 * W * B)
tacc	(7.6846e – 04 * W + 3.1334e – 02 * B + 1.4519e – 01 * S + 3.0153e – 01 * 0.02 * SL + 2.4784)
	Y = 16
mincyc	(2.0034e – 03 * W + 6.1934e – 02 * B + 2.3100e – 01 * 0.02 * SL + 3.4424) * 1.1
minckh	(3.1497e – 04 * W + 3.2373e – 02 * B + 6.2668e – 01 * 0.02 * SL + 2.0565)
minckl	(4.1660e – 04 * W + 4.5650e – 02 * B + 1.6429 + 9.4074e – 07 * W * B)
tacc	(3.8423e – 04 * W + 6.2668e – 02 * B + 1.4519e – 01 * S + 3.0153e – 01 * 0.02 * SL + 2.4784)
	Y = 32
mincyc	(1.0017e – 03 * W + 1.2386e – 01 * B + 2.3100e – 01 * 0.02 * SL + 3.4424) * 1.1
minckh	(1.5092e – 04 * W + 5.2514e – 02 * B + 7.0162e – 01 * 0.02 * SL + 2.4402)
minckl	(2.0830e – 04 * W + 9.1300e – 02 * B + 1.6429 + 9.4073e – 07 * W * B)
tacc	(1.9211e – 04 * W + 1.2533e – 01 * B + 1.4519e – 01 * S + 3.0153e – 01 * 0.02 * SL + 2.4784)

2) Power Characteristics [Unit: μW]

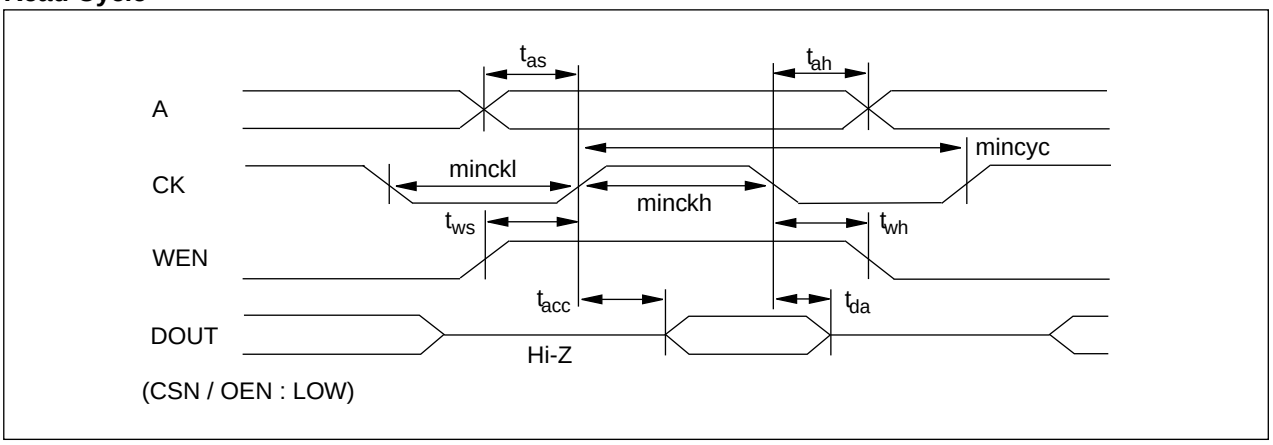
Power Type	Power Equation
	Y = 2
power_ck	(1.9286e – 01 * W + 1.2120 * B + 6.6767 + 1.0122e – 03 * W * B) * VDD^2 * F
power_csn	(1.4833e – 02 * W + 2.7771e – 01 * B + 6.7137e – 01 – 1.3698e – 04 * W * B) * VDD^2 * F
	Y = 4
power_ck	(9.6430e – 02 * W + 2.4241 * B + 6.6767 + 1.0122e – 03 * W * B) * VDD^2 * F
power_csn	(7.4166e – 03 * W + 5.5542e – 01 * B + 6.7137e – 01 – 1.3698e – 04 * W * B) * VDD^2 * F
	Y = 8
power_ck	(4.5015e – 02 * W + 4.0033 * B + 6.9783 + 2.2423e – 03 * W * B) * VDD^2 * F
power_csn	(3.7083e – 03 * W + 1.1108 * B + 6.7137e – 01 – 1.3698e – 04 * W * B) * VDD^2 * F
	Y = 16
power_ck	(2.1634e – 02 * W + 6.4680 * B + 7.4439 + 2.6999e – 03 * W * B) * VDD^2 * F
power_csn	(1.8541e – 03 * W + 2.2216 * B + 6.7137e – 01 – 1.3698e – 04 * W * B) * VDD^2 * F
	Y = 32
power_ck	(1.0383e – 02 * W + 1.0897e + 01 * B + 9.5049 + 2.6458e – 03 * W * B) * VDD^2 * F
power_csn	(9.2708e – 04 * W + 4.4433 * B + 6.7137e – 01 – 1.3698e – 04 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

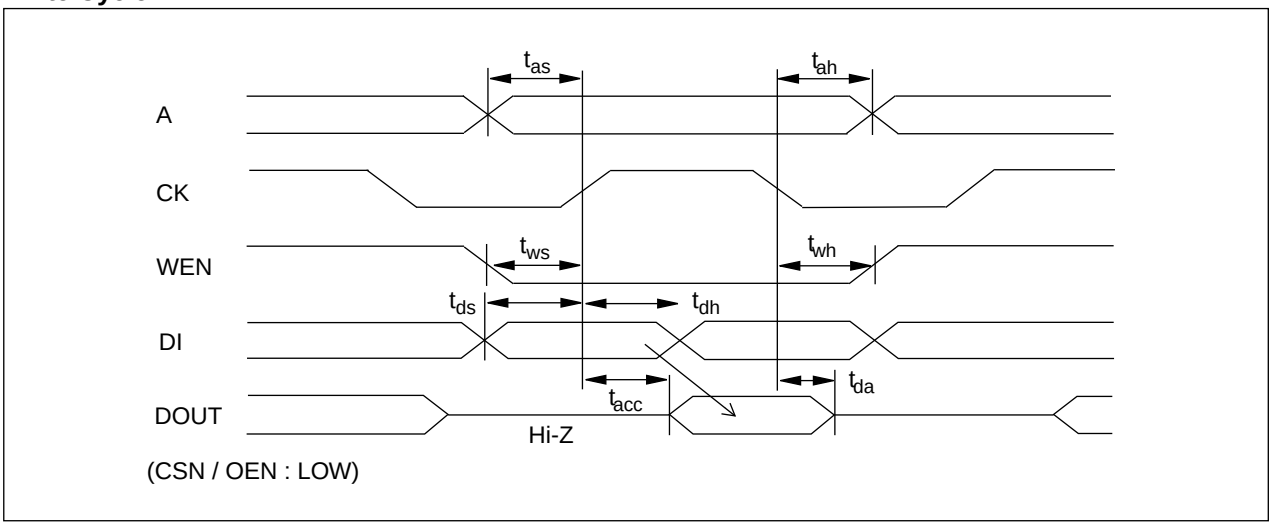
Width = 16.6 * ($\lceil \log_2 (W / Y) \rceil$) + 12.1 * B * Y + 121.7 [μm]
Height = 404.95 + 10.85 * W / Y + M [μm]
M = 8.15 (if Y = 2, 8), M = 10.55 (if Y = 4, 16), M = 12.95 (if Y = 32)

Timing Diagrams

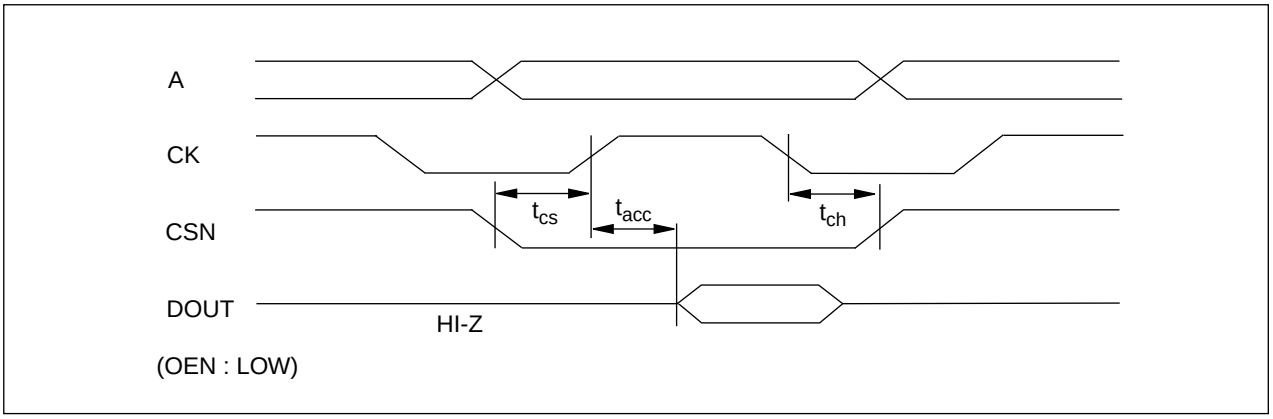
Read Cycle



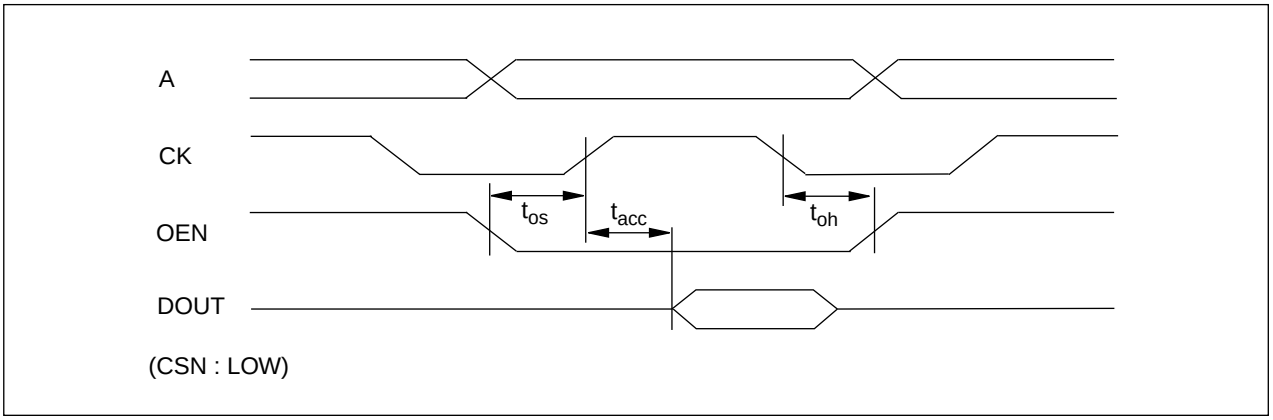
Write Cycle



CSN Control

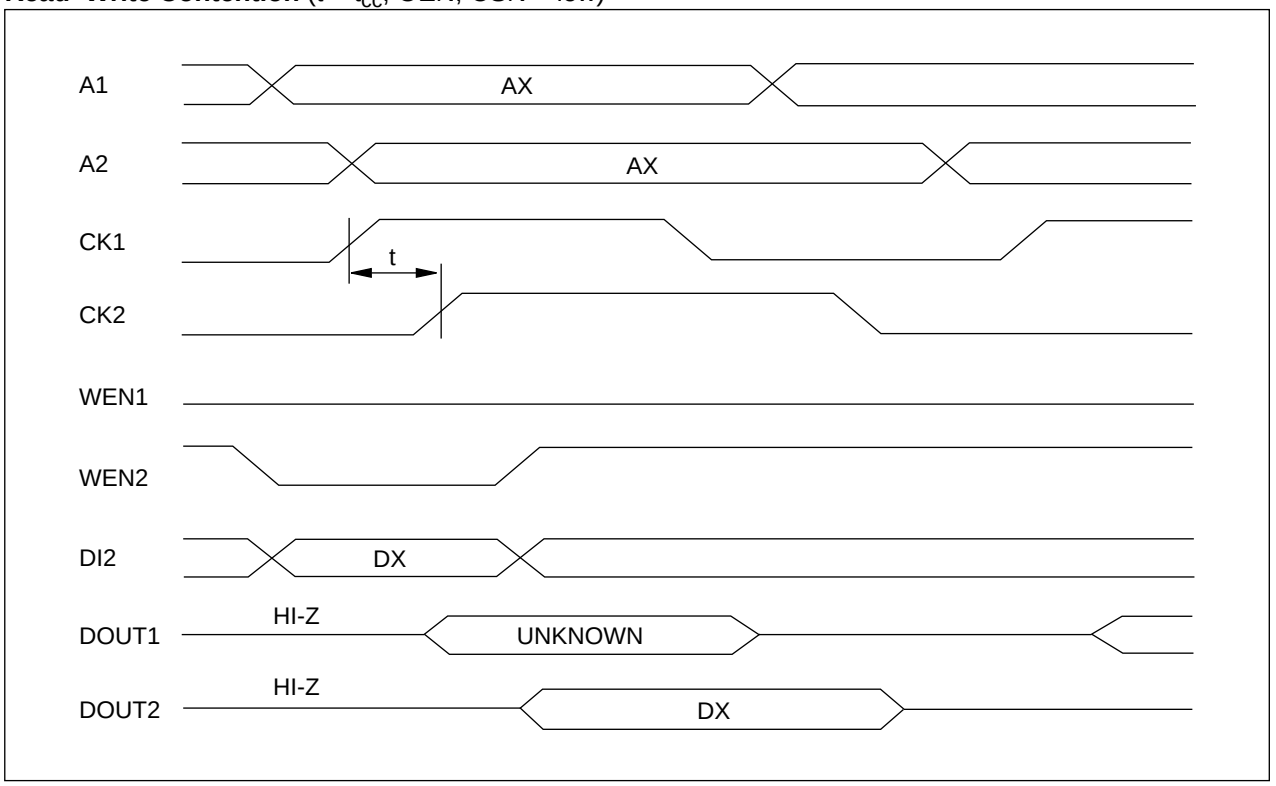


OEN Control

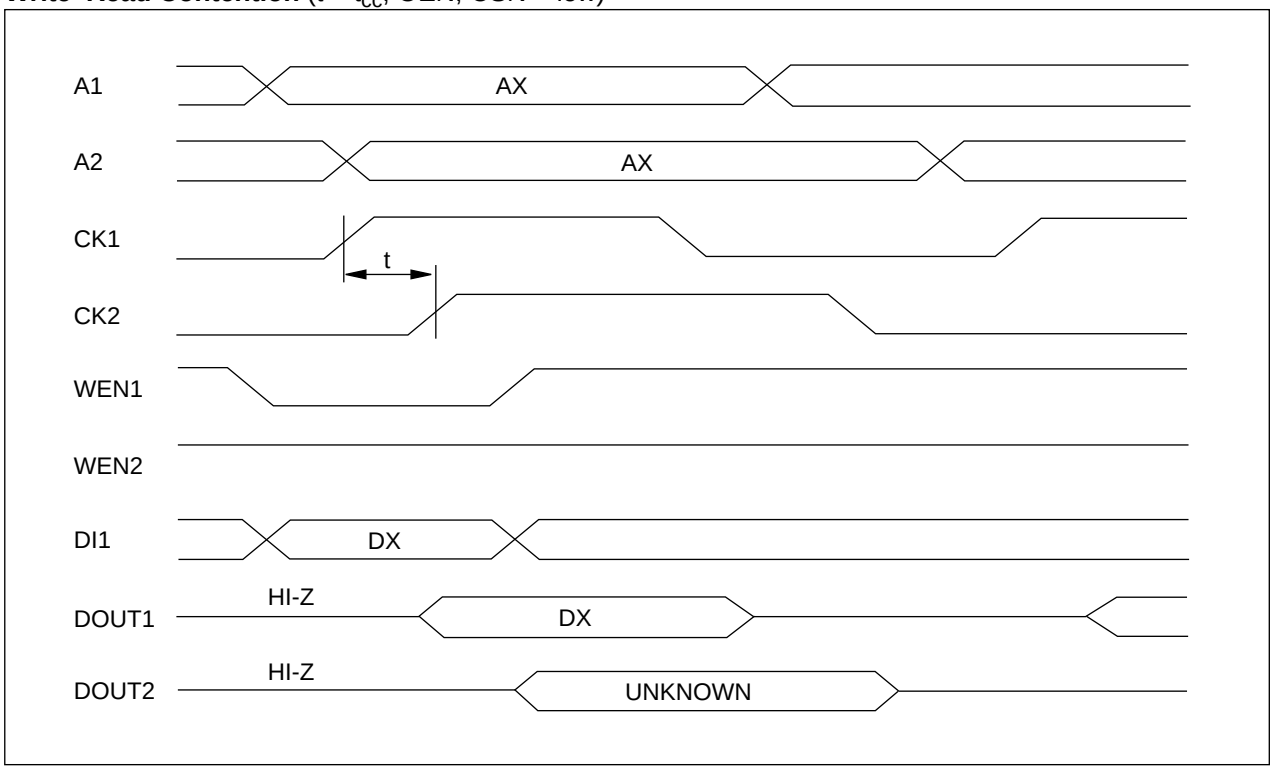


Function Diagrams

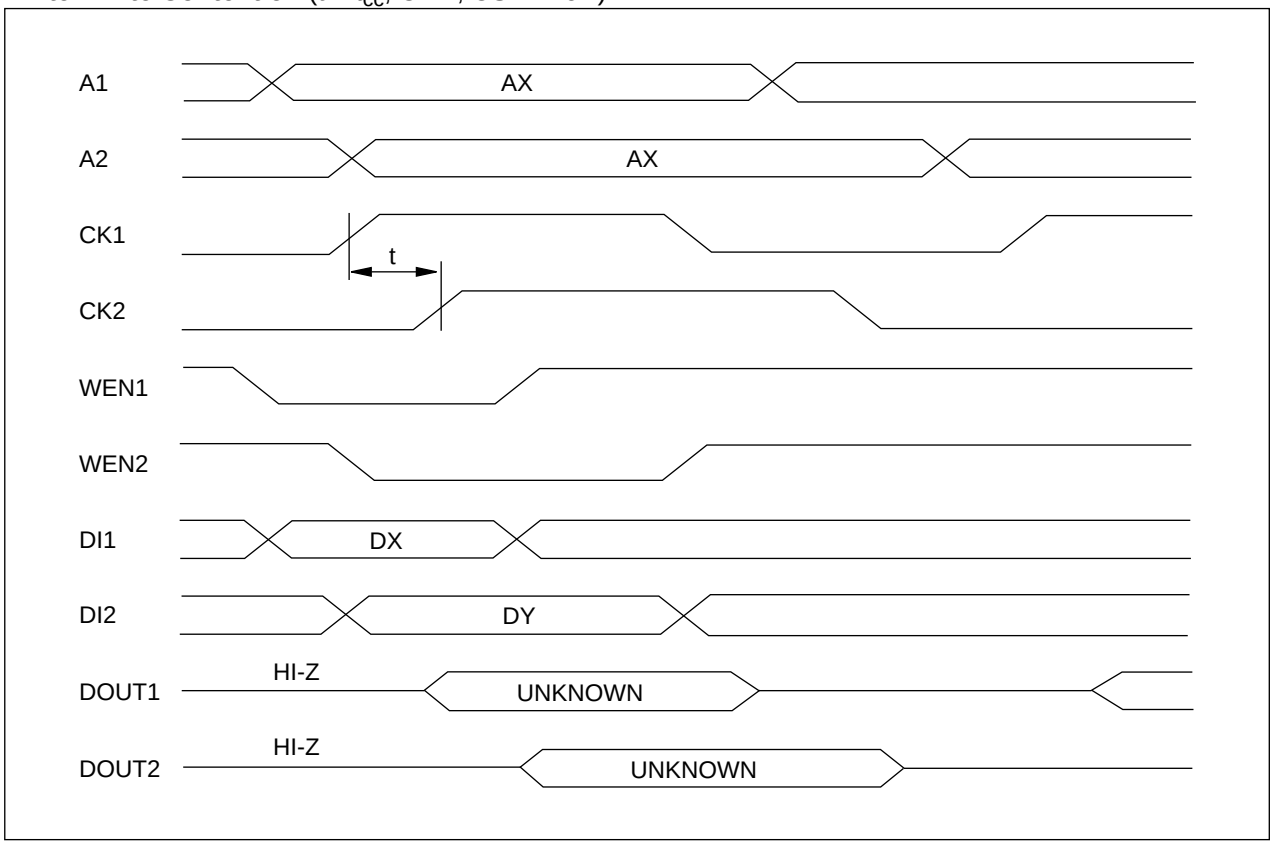
Read–Write Contention ($t < t_{cc}$; OEN, CSN = low)



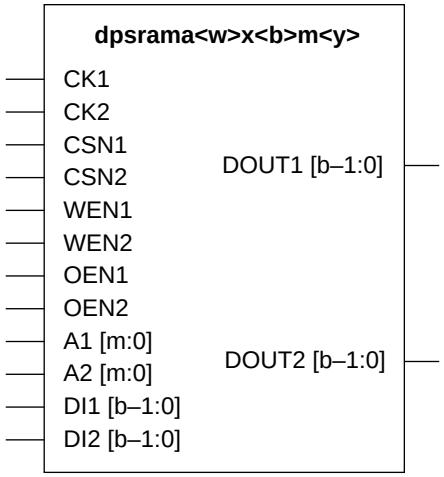
Write–Read Contention ($t < t_{cc}$; OEN, CSN = low)



Write–Write Contention (t < t_{cc}; OEN, CSN = low)



Logic Symbol



NOTES:

1. Words (w) is the number of words in DPSRAMA.
2. Bpw (b) is the number of bits per word.
3. Ymux (y) is one of the lower address decoder types.
4. $m = \lceil \log_2 w \rceil - 1$

Features

- Synchronous operation
- Read initiated at rising edge of clock
- Write completed at falling edge of clock
- Possible read modified write cycle
- Stand-by (power down) mode available
- Tri-state output
- Separated data I/O
- Low noise output circuit
- Possible bi-directional operation
- Flexible aspect ratio
- Up to 64K bits capacity
- Up to 8K number of words
- Up to 128 number of bits per word

Function Description

DPSRAMA is a dual-port synchronous static RAM. When WEN1 is high and CK1 rises, DOUT1 [ ] presents data stored in the location addressed by A1 [ ]. When WEN1 is low and CK1 falls, or when CK1 is high and WEN1 rises, the value of DI1 [ ] is written into the location addressed by A1 [ ]. CSN1 is used to enable/disable CK1. OEN1 is used to enable/disable tri-state drivers of DOUT1 [ ]. The functionality of port2 is the same to port1. The port1 and port2 function independently each other.
DPSRAMA is an alternative of DPSRAM. The major difference of these two RAMs is the timing of read and write. DPSRAMA reads and writes at different edge of the clock since DPSRAM reads and writes at the same edge of the clock.

Generators and Cell Configurations

DPSRAMA Gen. generates layout, netlist, symbol and functional & timing model of DPSRAMA. The layout of DPSRAMA is an automatically generated array of custom, pitch-matched leaf cells. To customize the configuration of DPSRAMA, you can give certain values to following three generator parameters:

- Number of words (w)
- Number of bits per word (b)
- Lower address decoder type (y).

The valid range of these parameters is specified in the following table:

Parameters		YMUX = 2	YMUX = 4	YMUX = 8	YMUX = 16	YMUX = 32
Words (w)	Min	4	8	16	32	64
	Max	512	1024	2048	4096	8192
	Step	2	4	8	16	32
Bpw (b)	Min	1	1	1	1	1
	Max	128	64	32	16	8
	Step	1	1	1	1	1

Pin Descriptions

Name	I/O	Description
CK1 CK2	I	“Clock”s serve as input clocks to each port of the memory block. When CK1 (CK2) is low, port1 (port2) is in a precharge state. Upon the rising edge, a read cycle begins. Upon the falling edge, a write cycle ends.
CSN1 CSN2	I	“Chip Select Negative”s act as each port’s enable signal for selections of multiple blocks on a common clock. When CSN1 (CSN2) is high, port1 (port2) goes to stand-by (power down) mode and no access can occur, conversely, if low only then may a read or write access occur. CSN1 (CSN2) may not change during CK1 (CK2) is high.
WEN1 WEN2	I	“Write Enable Negative”s select the type of memory access. Read is the high state, and write is the low state.
OEN1 OEN2	I	“Output Enable Negative”s control the output drivers from driven to tri-state condition. OEN1 (OEN2) may not change during CK1 (CK2) is high.
A1 [ ] A2 [ ]	I	“Address”es select the location to be accessed. A1 [ ] (A2 [ ]) may not change during CK1 (CK2) is high.
DI1 [ ] DI2 [ ]	I	When CK1 (CK2) falls while WEN1 (WEN2) is low, or when WEN1 (WEN2) rises while CK1 (CK2) is high, the “Data In” word value is written to the accessed location.
DOUT1 [ ] DOUT2 [ ]	O	During a read access, data word stored will be presented to the “Data Out” ports. DOUT1 [ ] and DOUT2 [ ] are tri-statable. When CK1 (CK2) is high, CSN1 (CSN2) is low and OEN1 (OEN2) is low, only then, DOUT1 [ ] (DOUT2 [ ]) drives a certain value. Otherwise, DOUT1 [ ] (DOUT2 [ ]) keeps Hi-Z state. During a write access, the value of DOUT1 [ ] (DOUT2 [ ]) is unpredictable.

Pin Capacitance

(Unit = SL)

CK	CSN	WEN	OEN	A	DI	DOUT				
						Ymux 2	Ymux 4	Ymux 8	Ymux 16	Ymux 32
5.8	1.9	0.9	2.3	1.0	2.0	5.4	5.4	12.0	25.0	51.0

Application Notes

1) Putting Busholders on DOUT1 [ ] and DOUT2 [ ]

As you will see in the timing diagrams, DOUT1 [ ] (DOUT2 [ ]) is valid only when CK1 (CK2) is high. If you want DOUT1 [ ] (DOUT2 [ ]) to be stable regardless of CK1 (CK2) state, you should put STDL80 Busholder cells on the DOUT1 [ ] (DOUT2 [ ]) bus externally.

2) Customizing Aspect Ratio

Aspect ratio is programmable using low address decoder types. As you can see in the configuration table, there are up to 5 selections of Ymux for the same Words and the same Bpw DPSRAMA. You can choose one of them in accordance with your chip level layout preference. Larger Ymux means fatter and shorter aspect ratio and smaller Ymux means thinner and taller aspect ratio. As you can see in the characteristic tables, aspect ratio affects major characteristics of DPSRAM, In general, larger Ymux DPSRAMA has faster speed and bigger area than smaller Ymux DPSRAMA.

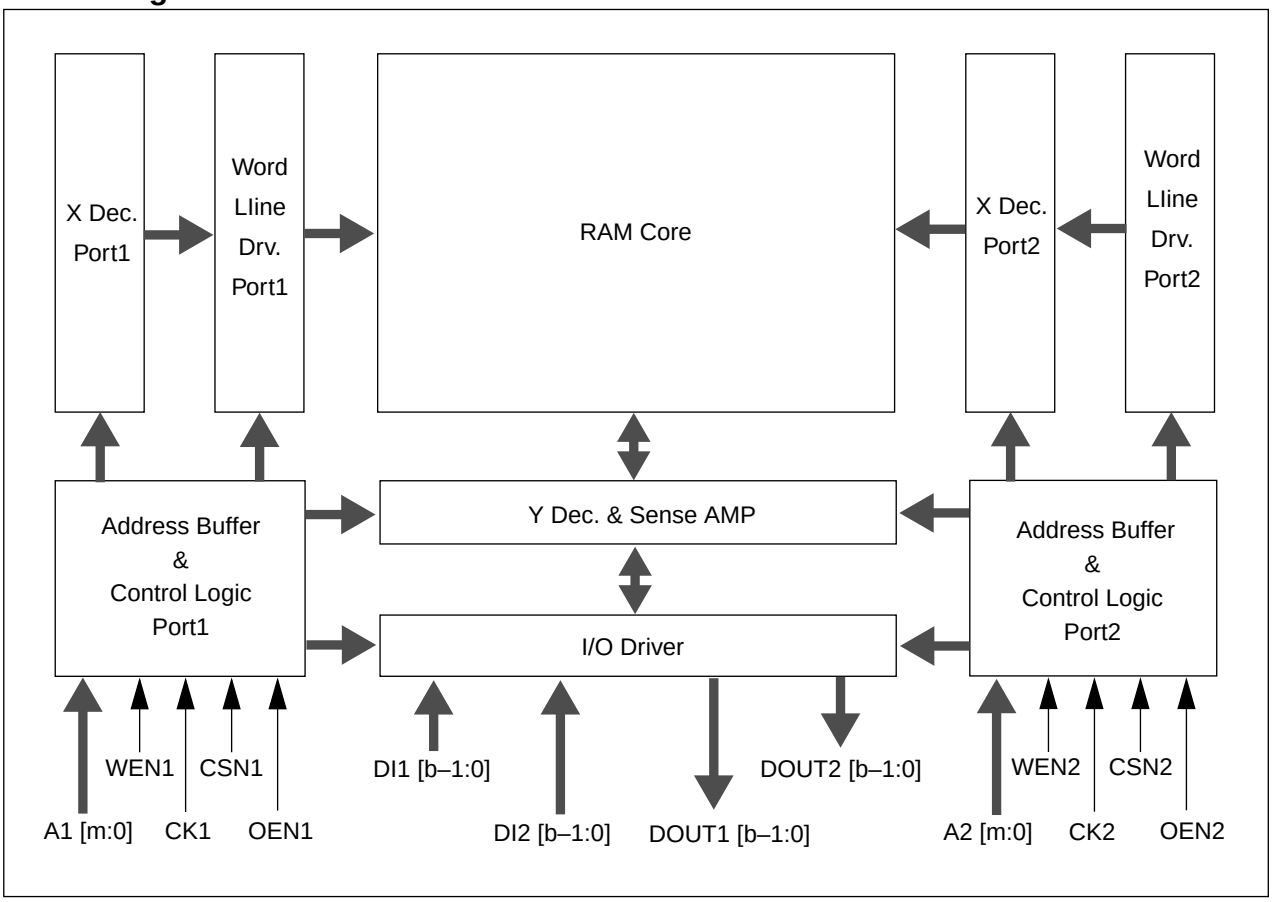
3) Contention Modes

Simultaneous accesses to the same location through both ports cause a contention. DPSRAMA has no contention preventing scheme. You have to take care of the contention modes. Please refer to the timing diagrams of contention modes to get more information of contention modes.

4) Using Bi-Directional Data Port

Because having the same phase, DI1 [ ] (DI2 [ ]) and DOUT1 [ ] (DOUT2 [ ]) of DPSRAMA can be tied directly. With tying them up together and controlling WEN1 (WEN2) and OEN1 (OEN2) properly, you can use them as bi-directional data ports.

Block Diagram



Characteristic Reference Table

Symbol	Description	256x16m4	1024x16m8	4Kx16m16
TIMING REQUIREMENTS & DELAY (Typical process, 3.3V, 25 ^{o}C, Output load = 10SL, Unit = ns)				
t_{rp}	Minimum Read Pulse Width	3.75	4.50	5.62
t_{pc}	Minimum Pre-Charge Period	5.12	6.06	12.50
t_{wp}	Minimum Write Pulse Width	1.63	2.35	4.48
t_{rwc}	Read-Write Contention	1.28	1.84	2.97
t_{wrc}	Write-Read Contention	0	0	0
t_{wwc}	Write-Write Contention	1.18	1.98	3.58
t_{as}	Address Setup Time	0.40	0.75	1.45
t_{ah}	Address Hold Time	1.20	2,05	3.75
t_{cs}	CSN Setup Time	0.70	0.70	0.70
t_{ch}	CSN Hold Time	0	0	0
t_{ds}	Data Input Setup Time	1.10	1.64	2.77
t_{dh}	Data Input Hold Time	1.30	1.58	2.21
t_{os}	OEN Setup Time	0	0	0
t_{oh}	OEN Hold Time	1.08	1.18	1.37
t_{wh}	WEN Hold Time	0.27	0.21	0.10
t_{acc}	Access Time	4.00	4.80	6.10
t_{da}	Deaccess Time	1.80	1.90	2.20
SIZE (µm)				
Width		996	1787	3353
Height		1110	1802	3194
POWER (µW/MHz)				
power_ck (normal mode: CSN Low)		1001	2249	6004
power_csn (stand-by mode: CSN High)		116	221	439

Characteristic Equation Tables

< Condition & Descriptions >

W: Number of Words
Y: Ymux Type
S: Input Slope (Unit: ns)
VDD: Operating Voltage (Unit: V)
B: Bits per Word
SL: Number of Fanouts (Unit: Standard Load)
F: Operating Frequency (Unit: MHz)

1) Timing Characteristics [Unit: ns]

Timing Type	Timing Equation
	Y = 2
tpc	1.59e – 02 * W – 4.37e – 03 * B – 4.90e – 01 * S + 2.2354 + 1.90e – 05 * W * B + 5.20e – 04 * W * S + 1.08e – 02 * B * S
trp	3.21e – 03 * W + 4.70e – 03 * B – 2.05e – 01 * S + 8.19e – 01 * 0.02 * SL + 2.5261
tacc	3.29e – 03 * W + 8.45e – 03 * B + 1.00e – 01 * S + 3.44e – 01 * 0.02 * SL + 2.3147
	Y = 4
tpc	7.99e – 03 * W – 8.74e – 03 * B – 4.90e – 01 * S + 2.2354 + 1.90e – 05 * W * B + 2.60e – 04 * W * S + 2.16e – 02 * B * S
trp	1.60e – 03 * W + 9.41e – 03 * B – 2.05e – 01 * S + 8.19e – 01 * 0.02 * SL + 2.5261
tacc	1.64e – 03 * W + 1.69e – 02 * B + 1.00e – 01 * S + 3.44e – 01 * 0.02 * SL + 2.3147
	Y = 8
tpc	3.99e – 03 * W – 1.74e – 02 * B – 4.90e – 01 * S + 2.2354 + 1.90e – 05 * W * B + 1.30e – 04 * W * S + 4.33e – 02 * B * S
trp	8.03e – 04 * W + 1.88e – 02 * B – 2.05e – 01 * S + 8.19e – 01 * 0.02 * SL + 2.5261
tacc	8.24e – 04 * W + 3.38e – 02 * B + 1.00e – 01 * S + 3.44e – 01 * 0.02 * SL + 2.3147
	Y = 16
tpc	1.99e – 03 * W – 3.49e – 02 * B – 4.90e – 01 * S + 2.2354 + 1.90e – 05 * W * B + 6.50e – 05 * W * S + 8.66e – 02 * B * S
trp	4.01e – 04 * W + 3.76e – 02 * B – 2.05e – 01 * S + 8.19e – 01 * 0.02 * SL + 2.5261
tacc	4.12e – 04 * W + 6.76e – 02 * B + 1.00e – 01 * S + 3.44e – 01 * 0.02 * SL + 2.3147
	Y = 32
tpc	9.99e – 04 * W – 6.99e – 02 * B – 4.90e – 01 * S + 2.2354 + 1.90e – 05 * W * B + 3.25e – 05 * W * S + 1.73e – 01 * B * S
trp	2.00e – 04 * W + 7.53e – 02 * B – 2.05e – 01 * S + 8.19e – 01 * 0.02 * SL + 2.5261
tacc	2.06e – 04 * W + 1.35e – 01 * B + 1.00e – 01 * S + 3.44e – 01 * 0.02 * SL + 2.3147

2) Power Characteristics [Unit: μW]

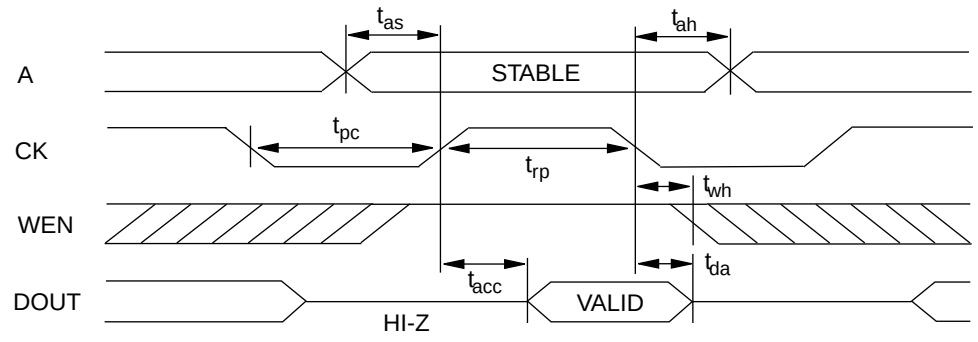
Power Type	Power Equation
	Y = 2
power_ck	(1.5772e – 01 * W + 1.1458 * B + 1.5858e + 01 + 4.7004e – 03 * W * B) * VDD^2 * F
power_csn	(9.2587e – 03 * W + 2.5036e – 01 * B + 1.3734 + 3.4497e – 05 * W * B) * VDD^2 * F
	Y = 4
power_ck	(7.8864e – 02 * W + 2.2916 * B + 1.5858e + 01 + 4.7004e – 03 * W * B) * VDD^2 * F
power_csn	(4.6293e – 03 * W + 5.0073e – 01 * B + 1.3734 + 3.4497e – 05 * W * B) * VDD^2 * F
	Y = 8
power_ck	(3.9432e – 02 * W + 4.5833 * B + 1.5858e + 01 + 4.7004e – 03 * W * B) * VDD^2 * F
power_csn	(2.3146e – 03 * W + 1.0014 * B + 1.3734 + 3.4497e – 05 * W * B) * VDD^2 * F
	Y = 16
power_ck	(1.9716e – 02 * W + 9.1667 * B + 1.5858e + 01 + 4.7004e – 03 * W * B) * VDD^2 * F
power_csn	(1.1573e – 03 * W + 2.0029 * B + 1.3734 + 3.4497e – 05 * W * B) * VDD^2 * F
	Y = 32
power_ck	(9.8581e – 03 * W + 1.8333e + 01 * B + 1.5858e + 01 + 4.7004e – 03 * W * B) * VDD^2 * F
power_csn	(5.7867e – 04 * W + 4.0058 * B + 1.3734 + 3.4497e – 05 * W * B) * VDD^2 * F

3) Size Equation [Unit: μm]

Width = 16.6 * ($\lceil \log_2 (W / Y) \rceil$) + 12.1 * B * Y + 121.7 [μm]
Height = 404.95 + 10.85 * W / Y + M [μm]
M = 8.15 (if Y = 2, 8), M = 10.55 (if Y = 4, 16), M = 12.95 (if Y = 32)

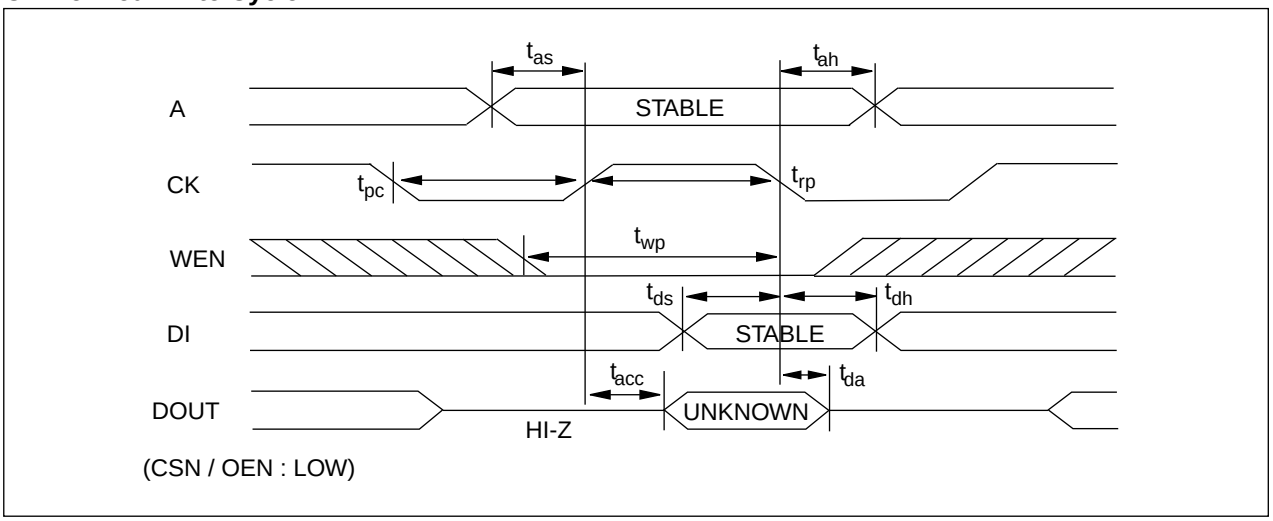
Timing Diagrams

Read Cycle

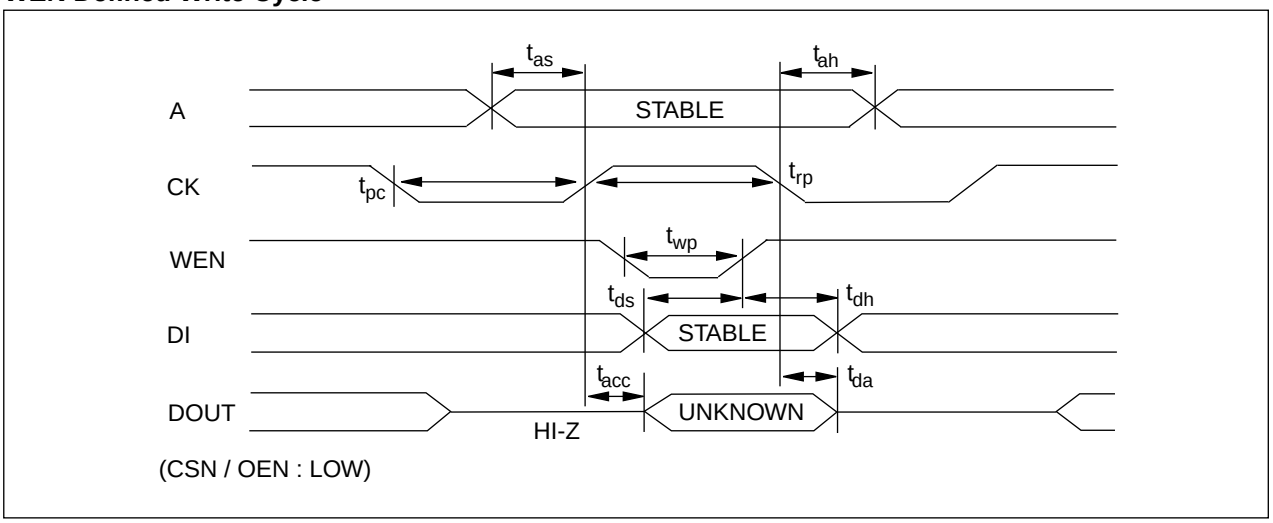


(CSN / OEN : LOW, DI :DON'T CARE)

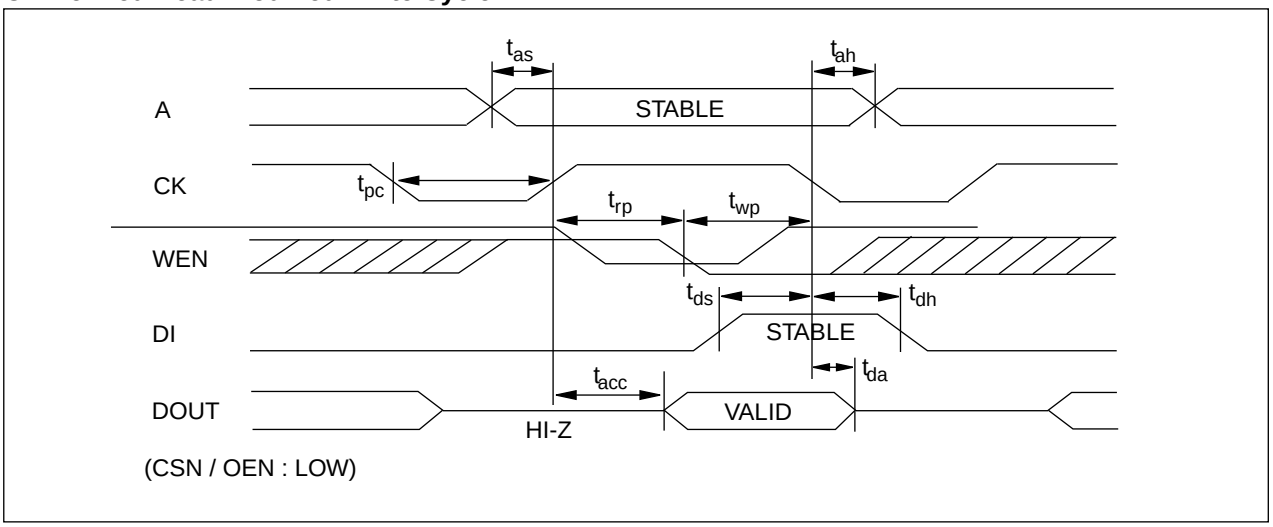
CK Defined Write Cycle



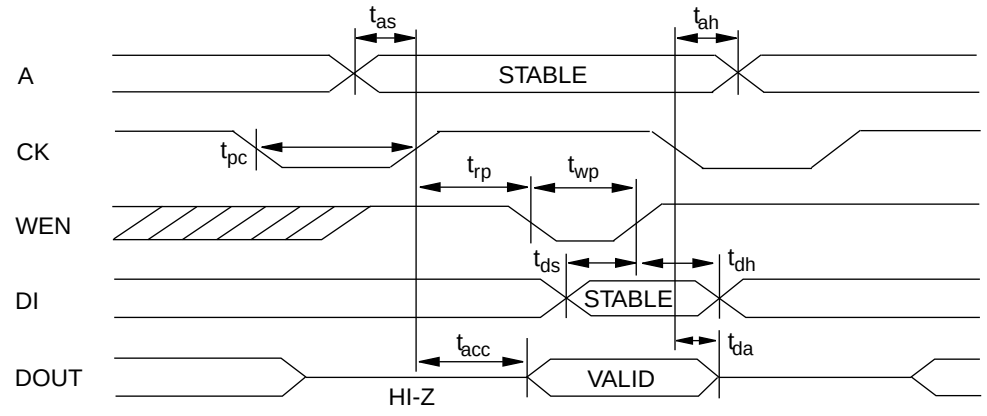
WEN Defined Write Cycle



CK Defined Read-Modified-Write Cycle

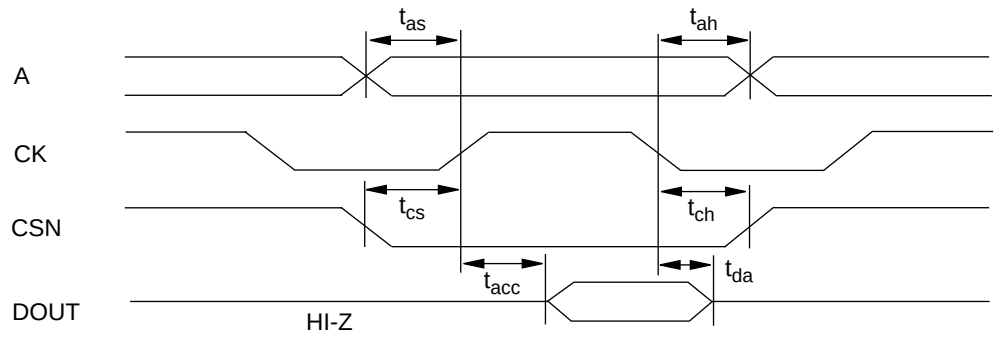


WEN Defined Read-Modified-Write Cycle



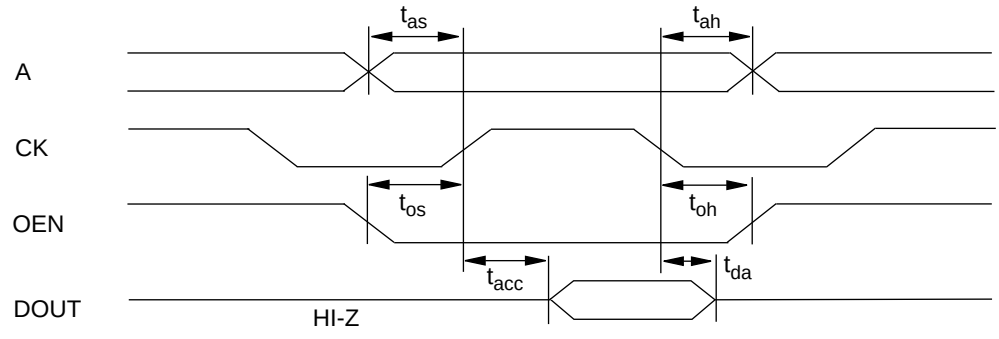
(CSN / OEN : LOW)

CSN Control



(OEN : LOW, WEN / DI : DON'T CARE)

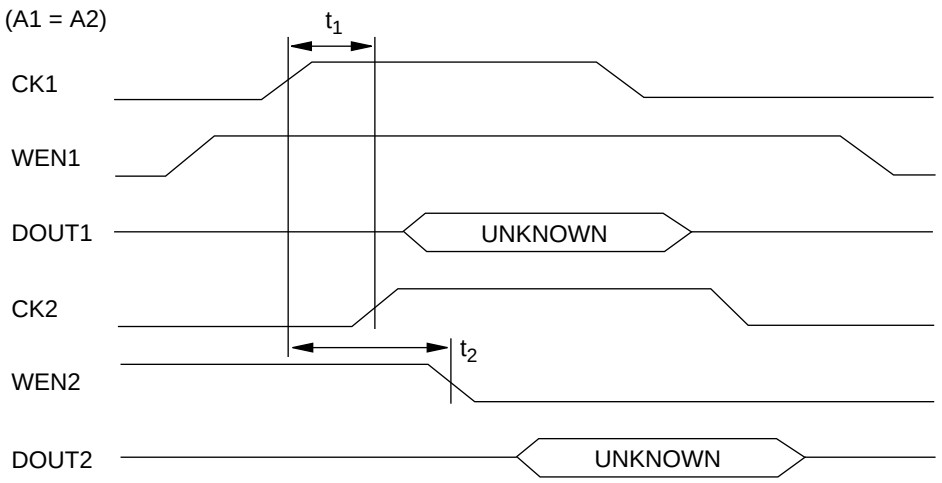
OEN Control



(CSN : LOW, WEN / DI : DON'T CARE)

Function Diagrams

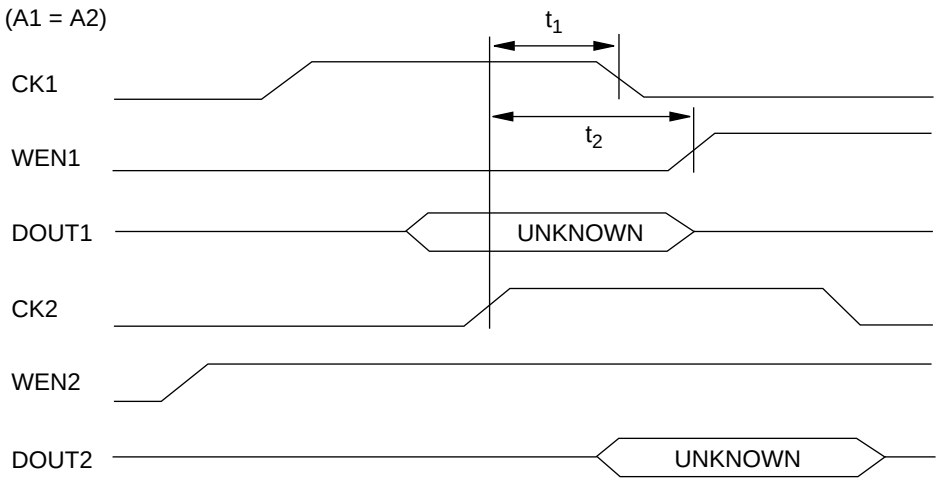
Read–Write Contention (max (t_1, t_2) ≤ t_{rwc})



(CSN1 / CSN2 / OEN1 / OEN2 : LOW, DI1 : DON'T CARE, DI2 : VALID)

* If the greater of t_1 or t_2 is smaller than or equal to t_{rwc}, it is Read-Write Contention.
The read by port1 is invalid, the write by port2 is still valid.

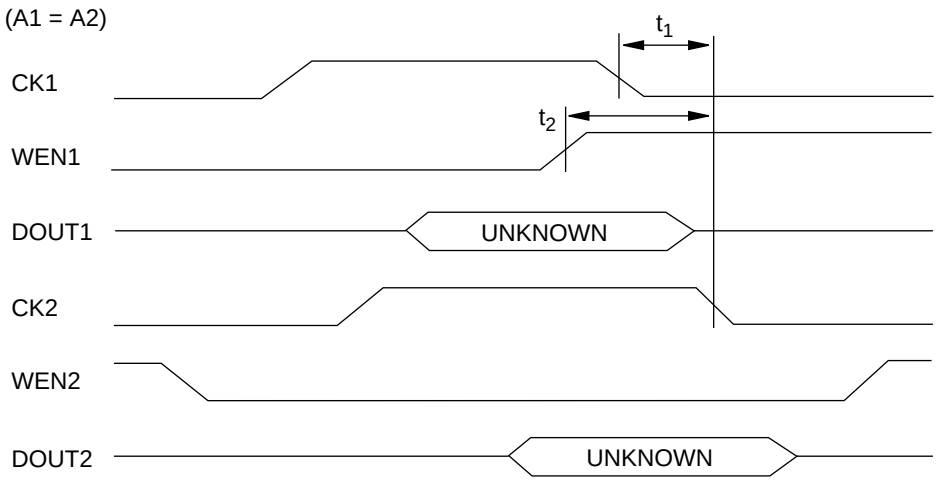
Write–Read Contention (min (t_1, t_2) ≥ t_{wrc})



(CSN1 / CSN2 / OEN1 / OEN2 : LOW, DI1 : VALID, DI2 : DON'T CARE)

* If the smaller of t_1 or t_2 is greater than or equal to t_{wrc}, it is Write-Read Contention.
The read by port2 is invalid, the write by port1 is still valid.

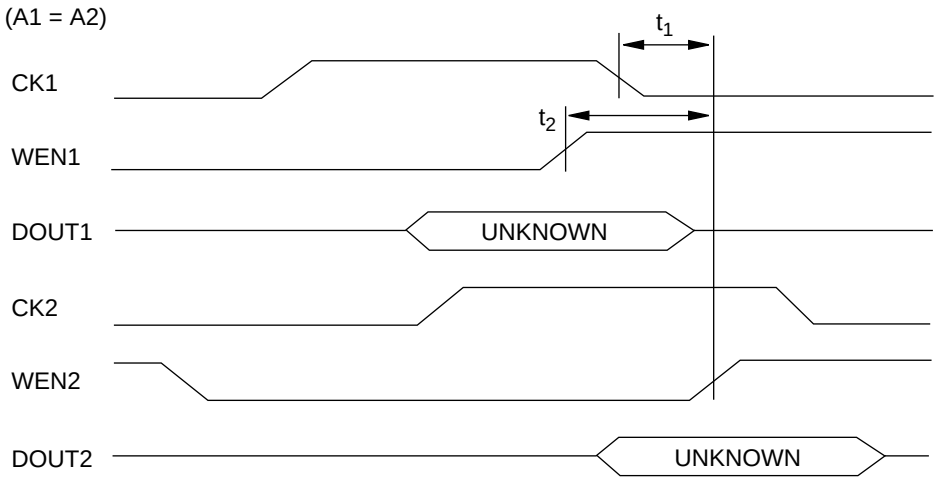
Write–Write Contention (max (t_1, t_2) ≤ t_{wwc} at CK Defined Write Cycle)



(CSN1 / CSN2 / OEN1 / OEN2 : LOW, DI1 / DI2 : VALID)

* If the greater of t_1 or t_2 is smaller than or equal to t_{wwc}, it is Write-Write Contention. Data stored at current address will be unpredictable.

Write–Write Contention (max (t_1, t_2) ≤ t_{wwc} at WEN Defined Write Cycle)



(CSN1 / CSN2 / OEN1 / OEN2 : LOW, DI1 / DI2 : VALID)

* If the greater of t_1 or t_2 is smaller than or equal to t_{wwc}, it is Write-Write Contention. Data stored at current address will be unpredictable.