Workshop on Compiler and Architectural Techniques for Application Reliability and Security (CATARS) – June 26th, 2008

Program at a glance

Session Title	Time
Session 1: Architectural Techniques for Application Reliability and Security (Session Chair: Karthik Pattabiraman)	**9:00 AM to 10:30 AM**
Session 2: Compiler Techniques for Application Reliability and Security (Session Chair: Shuo Chen)	**11:00 AM to 12:30 PM**
Session 3: Panel discussion on "Towards fault- and attack- resilient applications: where processor architects and compiler designers should converge"	**2:00 PM to 3:30 PM**

Detailed Program

Session 1: Architectural Techniques for Application Reliability and Security (9:00 A-10:30 A)

Session Chair: Karthik Pattabiraman

Towards Transient Fault Tolerance for Heterogeneous Computing Platforms, Nishant George, John Lach and Sudhanva Gurumurthi, *University of Viriginia (UVA)*

IOTA: Detecting Erroneous I/O Behavior via I/O Transaction Auditing, Albert Meixner and Daniel J. Sorin, *Duke University*

Using Open Compilation to Simplify the Design of Fault-Tolerant VLSI Systems, Juan-Carlos Ruiz, David de Andrés, Pedro Gil and Sara Blanc, *Universidad Politécnica de Valencia (UPV)*

Session 2: Compiler Techniques for Application Reliability and Security (11:00 A-12:30 P)

Session Chair: Shuo Chen

Count&Check: Counting Instructions to Detect Incorrect Paths, Long Wang and Ravishankar K. Iyer, *University of Illinois at Urbana-Champaign (UIUC)*

Reverse Stack Execution in a Multi-Variant Execution Environment, Babak Salamat, Andreas Gal and Michael Franz, *University of California, Irvine (UCI)*

Intrusion Detection via Instrumented Software, William Mahoney and William Sousan, *University of Nebraska at Omaha (UNO)*

Session 3: Panel Discussion on "Towards fault- and attack- resilient applications: where processor architects and compiler designers should converge" (2:00 P – 3:30 P)

Moderator: Zbigniew Kalbarczyk, **Panelists:** Subhasish Mitra (Stanford University), Brendan Murphy (Microsoft Research), Calton Pu (Georgia Institute of Technology) and Mohan Rajagopalan (Intel)